DDR5/LPDDR5 Test Challenges and Insight of Gen 6

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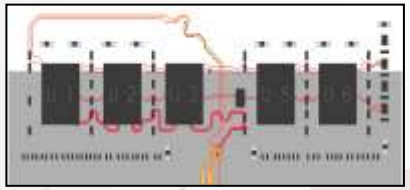
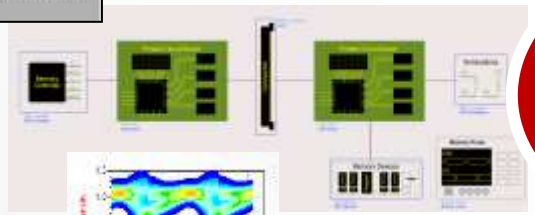
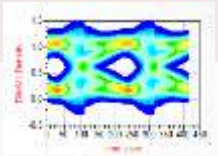
DDR5 Test Solutions








DDR Signal Evolution

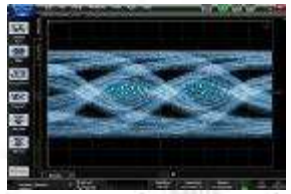
Speed | **Signal** | **Specification**

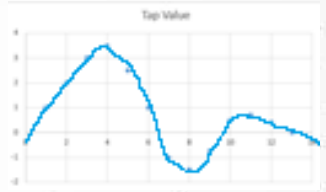
3200 – 6400 MT/s

DDR5

"Hyper Speed" - No visible eye

- Pre/De-Emphasis



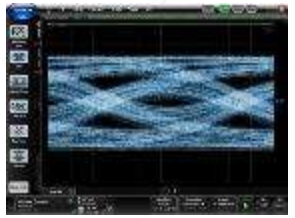


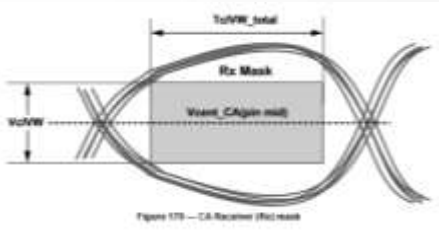
1600 – 4200 MT/s

DDR4

"Serial Speed" - Clock often embedded

- Eye Diagrams / Rx Masks
- Bit Error rates, Jitter / Noise





200 – 2133 MT/s

DDR3
DDR2
DDR

"High Speed" - Transmission lines

- Timing
- Impedance / load curves

SRAM

"Low Speed" - Auto place and route

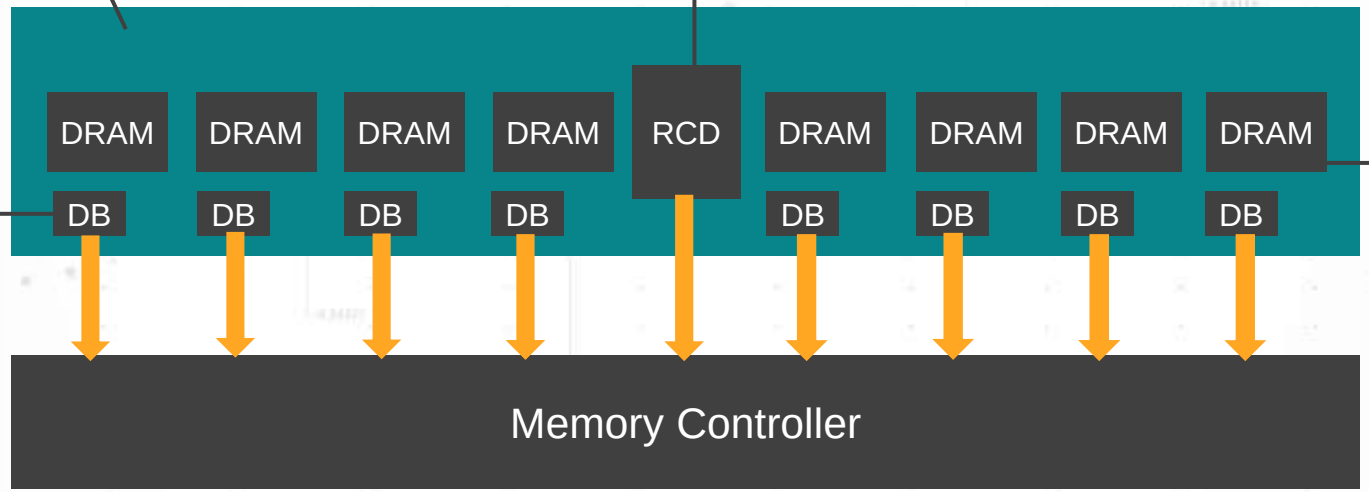
- Fanout
- Capacitance

DDR5 Devices

DIMM (RDIMM, LRDIMM, UDIMM, SODIMM)
- Rx test
- Protocol test

Register
- Rx test
- Tx test
- Protocol test

System Integrators
- Rx test
- Tx test
- Protocol test



Data Buffer
- Tx test
- Rx test
- Protocol test

DRAM
- Rx test
- Tx test
- Protocol test

DDR5 Tx Design Test and Validation

CHALLENGES AND SOLUTIONS

CHALLENGES

Signal integrity

Ensure interoperability

Time-to-market Pressure

SOLUTIONS

New definition of test parameters

Characterization and compliance test

The total solution approach

Design and Simulation | **Analysis and Debug** | **Compliance**

Data Analytics

Signal Integrity

NEW DEFINITION AND SPECIFICATION

New method to perform read and write data separation is required

- Legacy method to use DQS-DQ phase difference and pre-amble pattern may no longer be applicable

New test parameters are defined to characterize key signals operating at faster data rate

- Specification reveals tighter DQS, DQ, CK nUI jitter tests
- Duty Cycle Adjuster (DCA) optimized jitter measurements

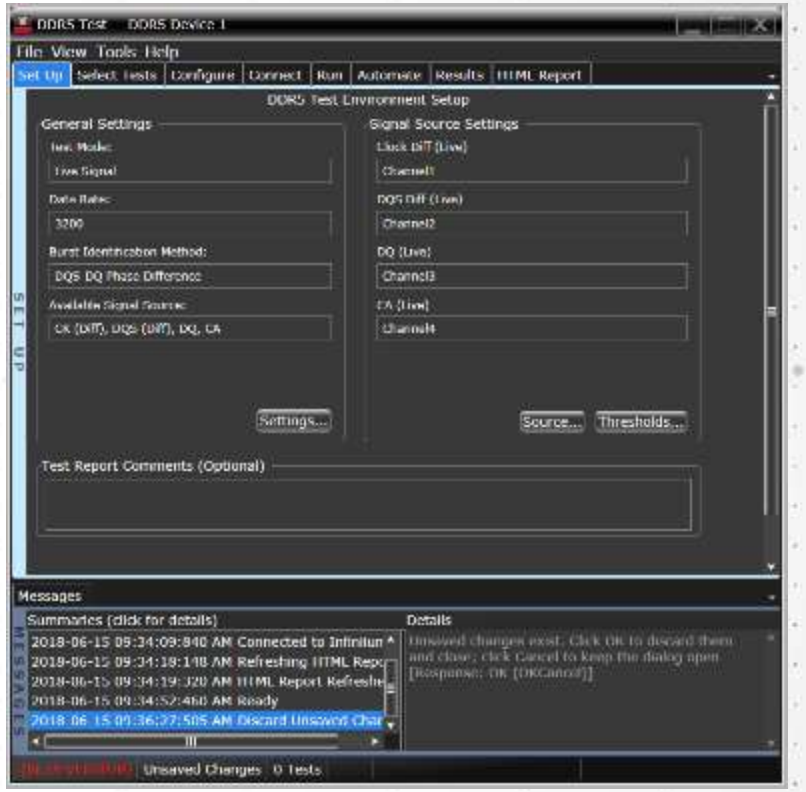
Faster data rate may cause data eye to close

- New method to characterize data is required
- Equalization may be required for speed above 3.6 GT/s

Ensuring Interoperability

CHARACTERIZATION AND COMPLIANCE TEST

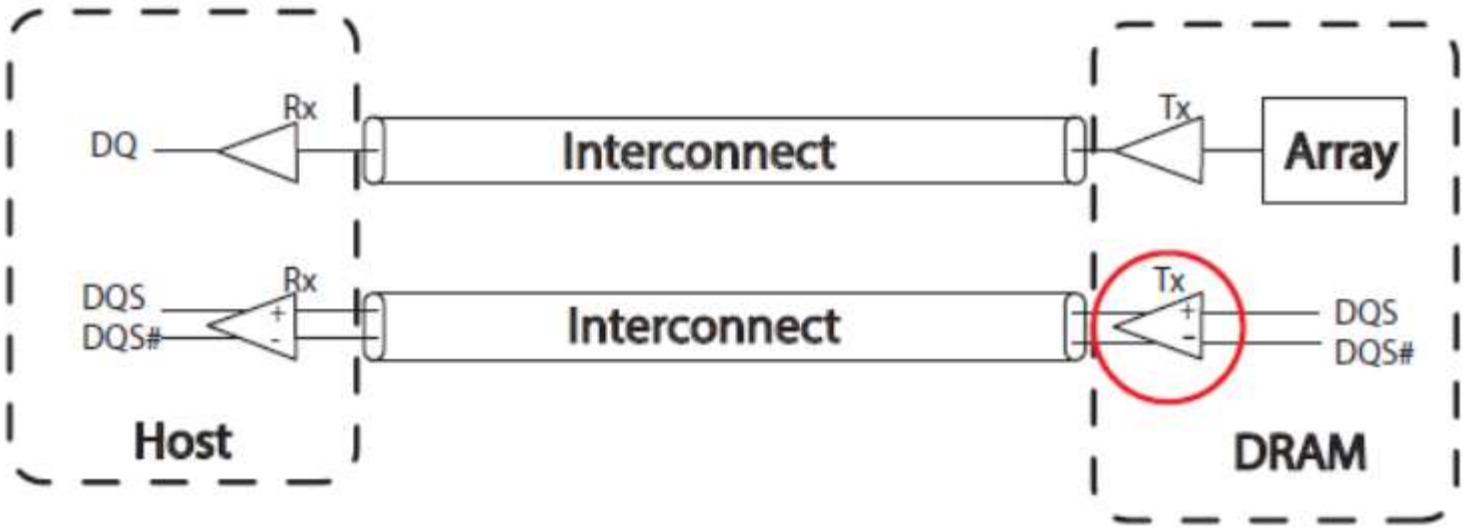
- Best high-performance oscilloscopes
- Complete test coverage:
  - Supports the latest DDR5 JEDEC spec
  - Speed bin from 3200 to 6400 MT/s
  - Supports electrical, timing, jitter and eye diagram tests
- Benefits:
  - Ensure interoperability between system and devices
  - Repeatability for accurate statistical analysis
  - Automation for speedy test time



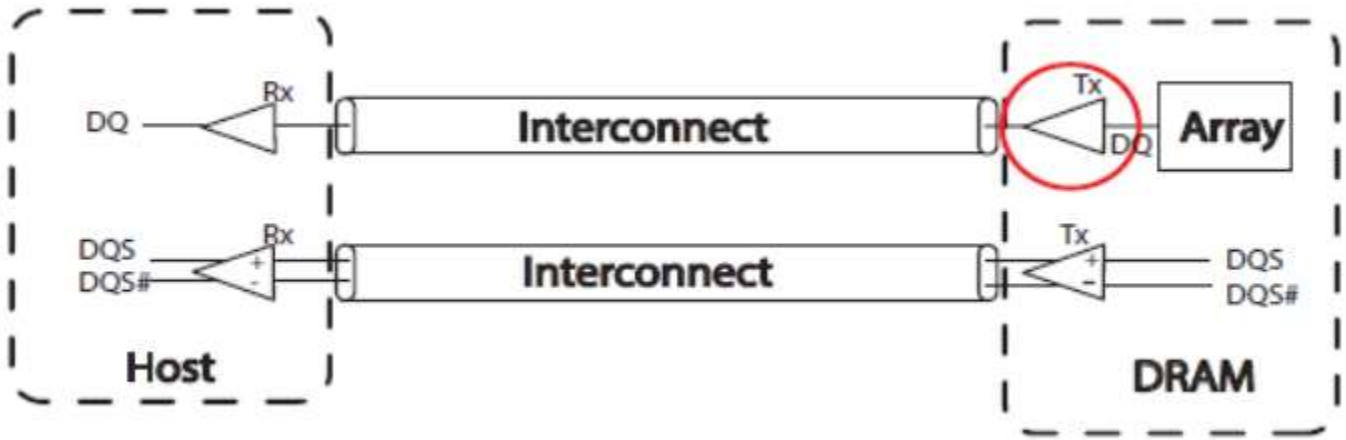
Design and Simulation | **Analysis and Debug** | **Compliance**

Data Analytics

Tx – New Specs



- tCK_NUI jitter (Dj Rj)
- DQS_NUI jitter (Dj Rj)
- DQ_NUI jitter (Dj Rj)
- DQ_Stressed Eye



Time to Market Pressure

THE TOTAL SOLUTION APPROACH

- Automated Compliance test for speedy test time
  - New algorithm for fast test time
- BGA interposer for easy access to signal for testing
  - Integrated Riser and Interposer for better performance
  - Easy attachment to DUT
- New ADS framework for completeness of simulation to validation workflow
- Seamless connection to data repository for quick test result analysis and decision making process

Design and Simulation

Analysis and Debug

Compliance

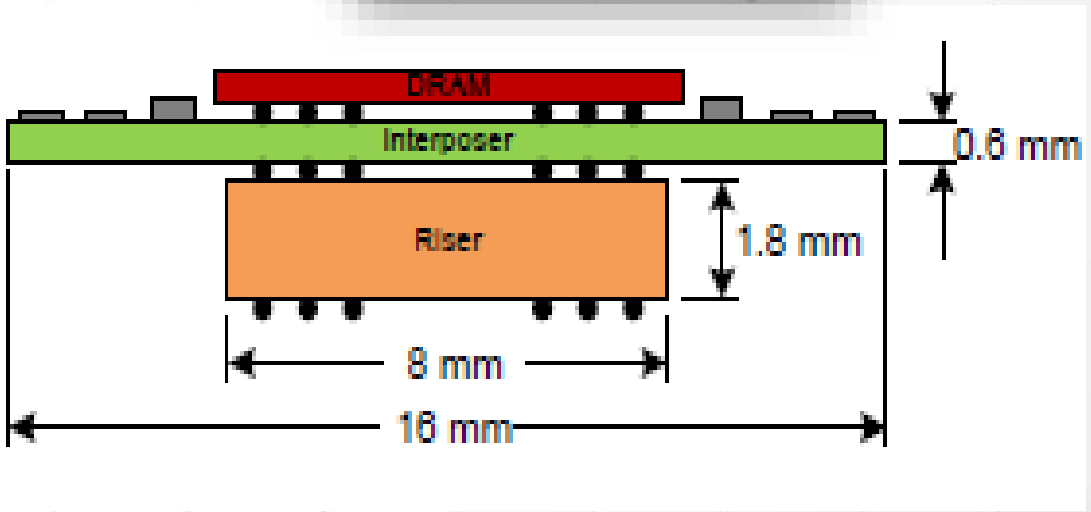
Data Analytics

Innovative Probing for DDR5

CRITICAL FOR THE TX SOLUTION

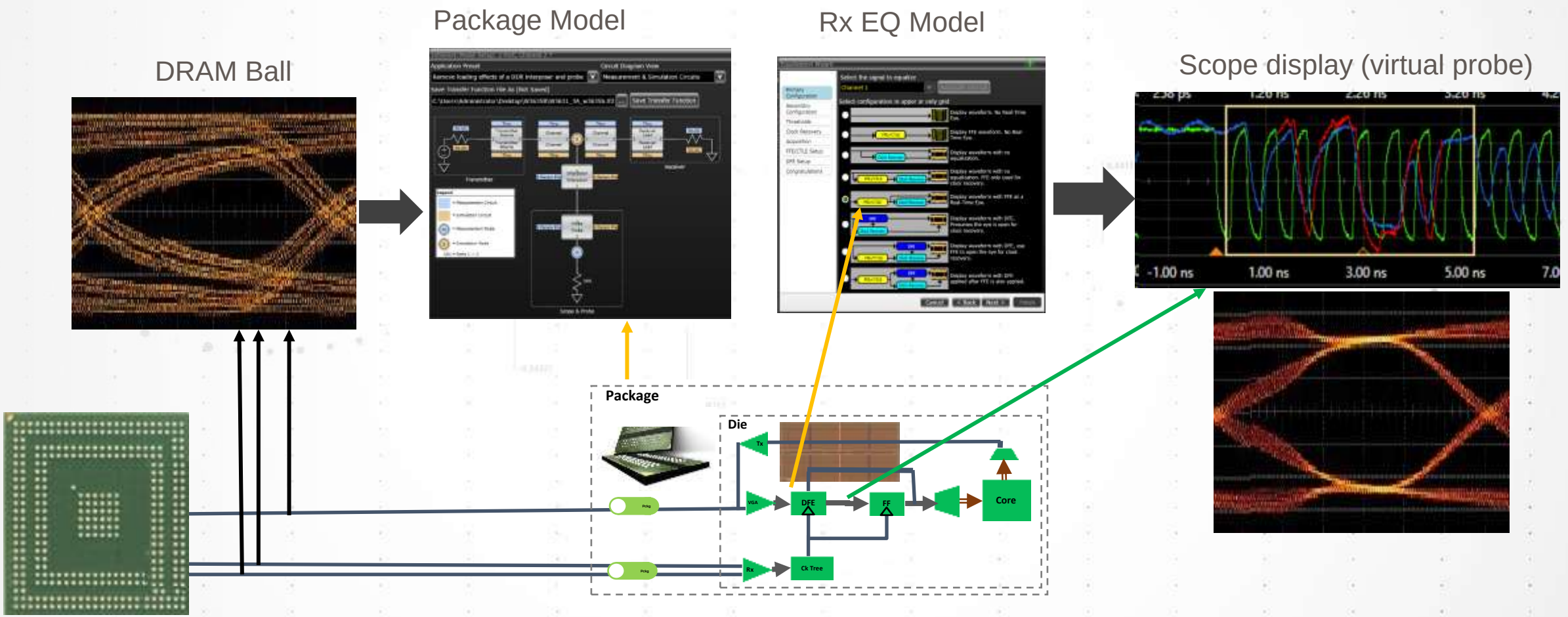
- InfiniiMax Ultra Series Probes
  - Lowest loading for least impact to your circuit
  - Higher density with 1/2 the size of existing solder-in probe heads
  - Highest accuracy across the widest frequency range

- DDR5 BGA Interposer
  - High performance SI interposer and riser
  - New riser designed to minimize crosstalk
  - High performance, low loss material



DDR5 Tx Test: New Methodology

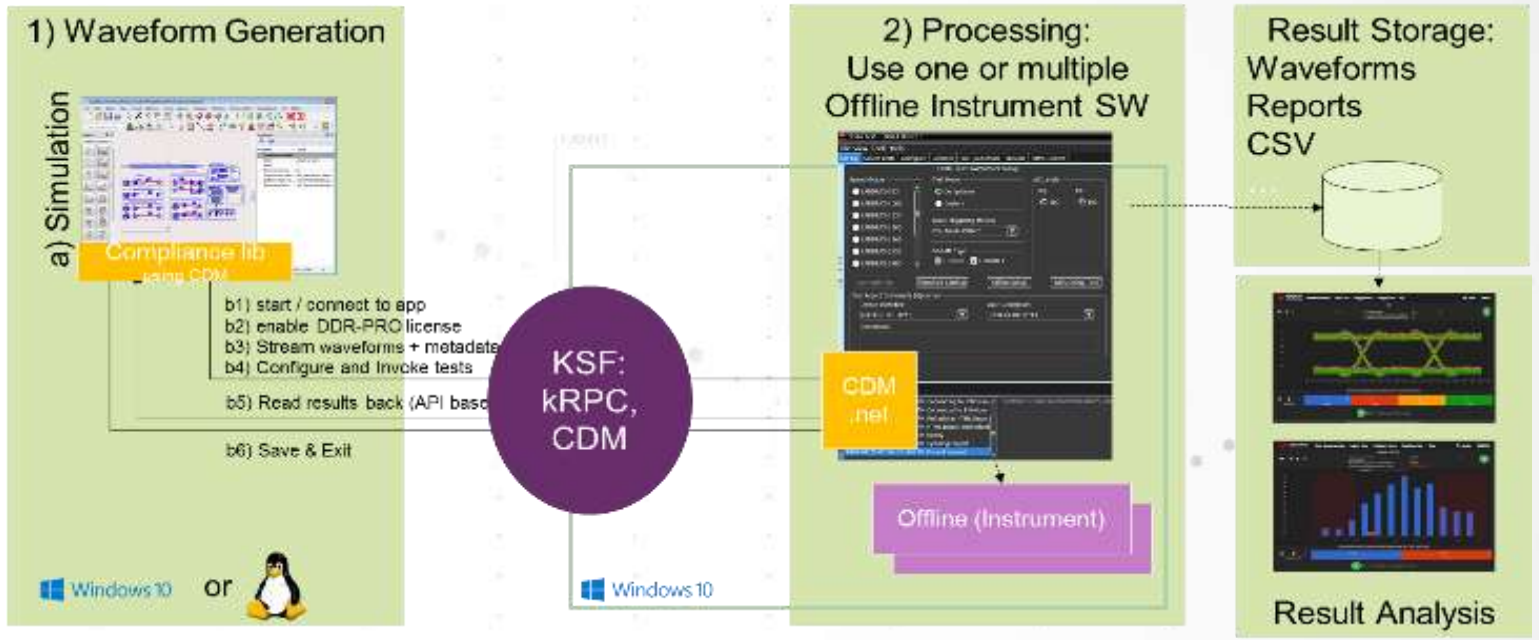
VIRTUAL PROBING INSIDE THE DIE



ADS Integration

INCREASE CONFIDENCE IN THE DESIGN

- Enable better-correlated compliance measurements - fewer surprises, shorter time to market.
  - Streamlined integration between ADS and Infiniium Offline with DDR5 compliance test app
  - ADS automates the configuration and control of the compliance test and receives measurement results back



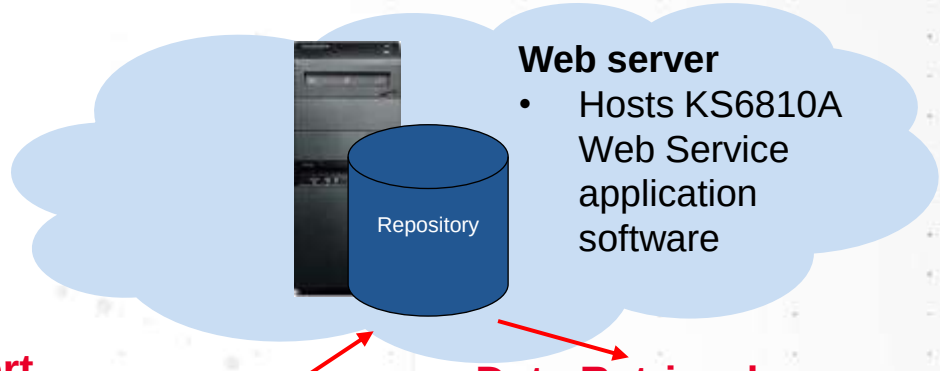
Design and Simulation | **Analysis and Debug** | **Compliance**

Data Analytics

Data Analytics

ENABLE SHORTER TIME TO MARKET

- Enables:
  - Save at least $1M chip redesign cost
  - Increase at least 20% in productivity
- Seamless connection to the KS6810A data analytics software
  - Offers enterprise class repository to store the data
  - Allows real time data retrieval with modern visualization tool

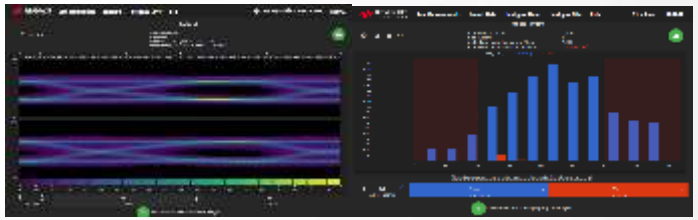


Data Import

- Test result with test condition

Data Retrieval

- KS6810A Web Visualization tool



Design and Simulation | **Analysis and Debug** | **Compliance**

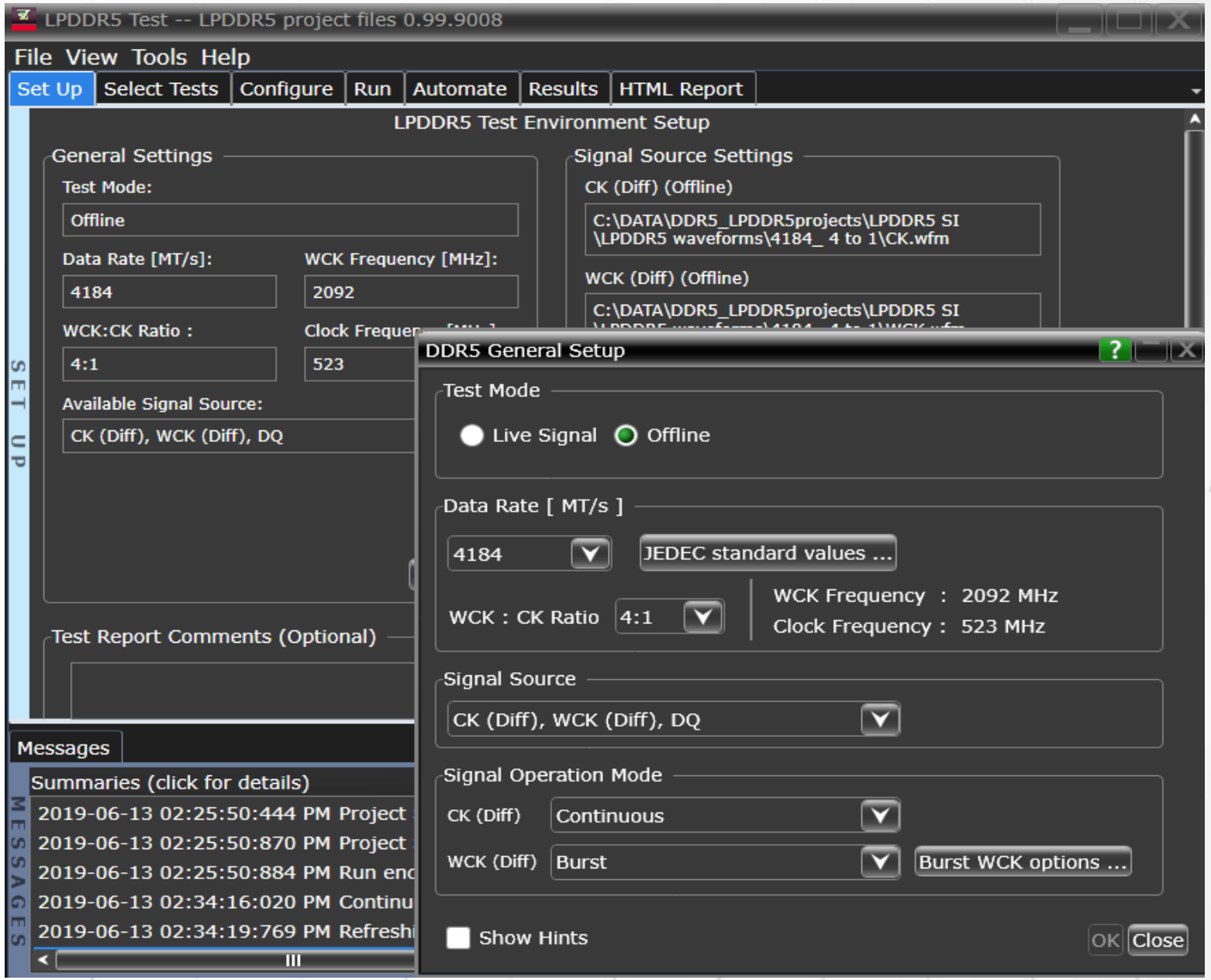
Data Analytics

Easy Test Setup

TX SOLUTION

LPDDR5 application test setup selections:

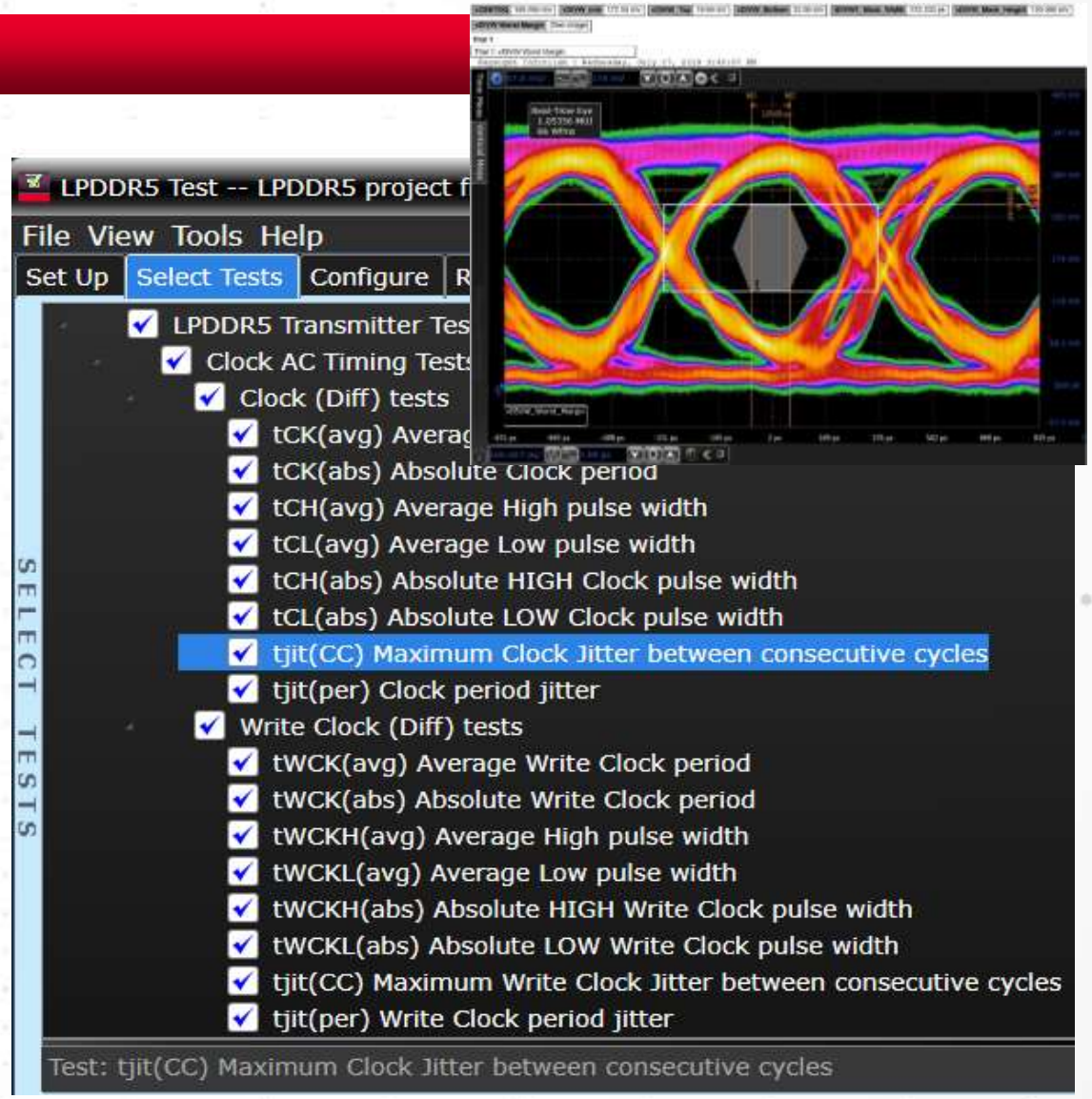
- Speed grade of device
- Live Signal or Off-line
- Signal sources



Configurability and Guided Connection

TX SOLUTION

- Select Tab lists tests available in the setup.
- Easily setup individual test or groups of tests.



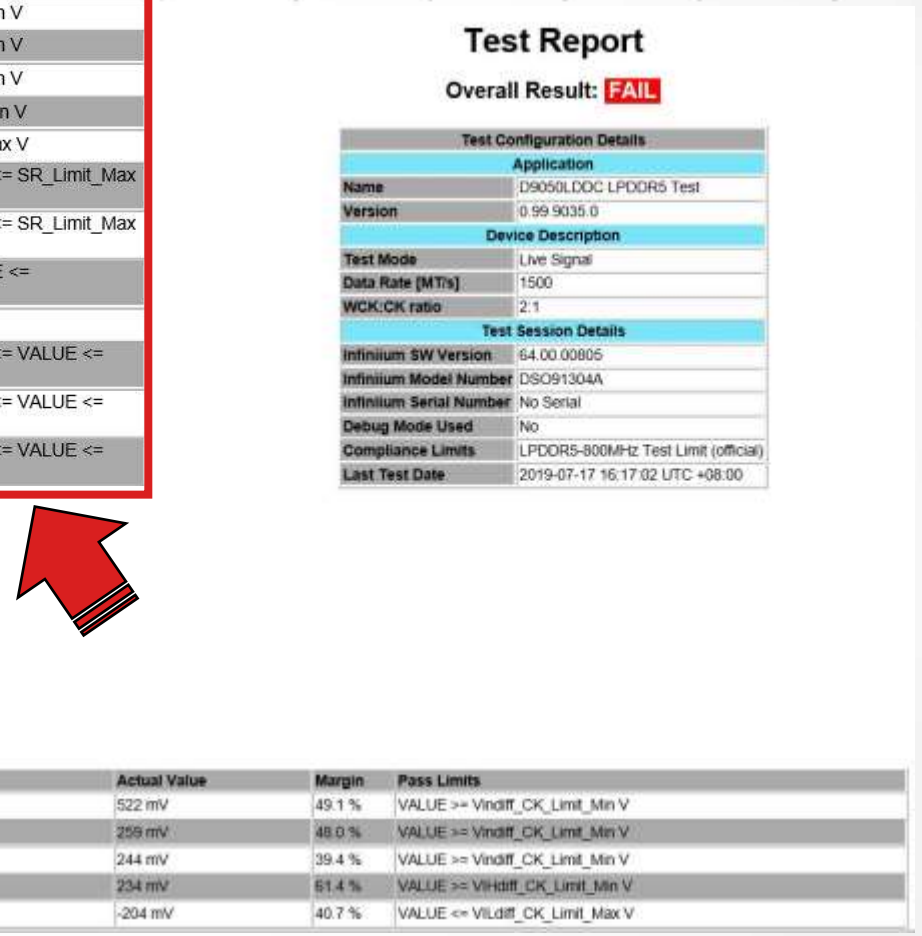
Comprehensive Compliance App Format and Features

TX SOLUTION

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	Vindiff_CK	1.745 V	398.6 %	VALUE >= Vindiff_CK_Limit_Min V
✓	0	1	Vindiff_CK/2HighPulse	894 mV	410.9 %	VALUE >= Vindiff_CK_Limit_Min V
✓	0	1	Vindiff_CK/2LowPulse	829 mV	373.7 %	VALUE >= Vindiff_CK_Limit_Min V
✓	0	1	VIHdiff_CK	728 mV	402.1 %	VALUE >= VIHdiff_CK_Limit_Min V
✓	0	1	VILdiff_CK	-785 mV	441.4 %	VALUE <= VILdiff_CK_Limit_Max V
✓	0	1	SRIdiffR_CK	4.814 V/ns	23.5 %	SR_Limit_Min V/ns <= VALUE <= SR_Limit_Max V/ns
✓	0	1	SRIdiffF_CK	2.211 V/ns	1.8 %	SR_Limit_Min V/ns <= VALUE <= SR_Limit_Max V/ns
✓	0	1	tCK(avg) Average Clock period	3.639 ns	0.6 %	tCK_avg_Limit_Min s <= VALUE <= tCK_avg_Limit_Max s
ⓘ		1	tCK(abs) Absolute Clock period	3.017 ns		Information Only
✓	0	1	tCH(abs) Absolute HIGH Clock pulse width	517.166290123 mtCK (avg)	37.7 %	tCHL_abs_Limit_Min tCK(avg) <= VALUE <= tCHL_abs_Limit_Max tCK(avg)
✓	0	1	tCH(avg) Average High pulse width	496.692500000 mtCK (avg)	45.9 %	tCHL_avg_Limit_Min tCK(avg) <= VALUE <= tCHL_avg_Limit_Max tCK(avg)
✗	1	1	tCL(abs) Absolute LOW Clock pulse width	338.559219496 mtCK (avg)	-65.3 %	tCHL_abs_Limit_Min tCK(avg) <= VALUE <= tCHL_abs_Limit_Max tCK(avg)

Test Report includes:

- Pass/Fail indicator, # of Trials
- Test Name, Actual value
- Margin
- Pass limits
- Image (where appropriate)



Test Report

Overall Result: FAIL

Test Configuration Details	
Application	
Name	D9050LDDC LPDDR5 Test
Version	0.99.9035.0
Device Description	
Test Mode	Live Signal
Data Rate [MT/s]	1500
WCK:CK ratio	2:1
Test Session Details	
Infiniium SW Version	64.00.00805
Infiniium Model Number	DSO91304A
Infiniium Serial Number	No Serial
Debug Mode Used	No
Compliance Limits	LPDDR5-800MHz Test Limit (official)
Last Test Date	2019-07-17 16:17:02 UTC +08:00

Summary of Results

Test Statistics	
Failed	2
Passed	30
Total	32

Margin Thresholds	
Warning	< 5 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	Vindiff_CK	522 mV	49.1 %	VALUE >= Vindiff_CK_Limit_Min V
✓	0	1	Vindiff_CK/2HighPulse	259 mV	48.0 %	VALUE >= Vindiff_CK_Limit_Min V
✓	0	1	Vindiff_CK/2LowPulse	244 mV	39.4 %	VALUE >= Vindiff_CK_Limit_Min V
✓	0	1	VIHdiff_CK	234 mV	61.4 %	VALUE >= VIHdiff_CK_Limit_Min V
✓	0	1	VILdiff_CK	-204 mV	40.7 %	VALUE <= VILdiff_CK_Limit_Max V

DDR5 Rx Design Test and Validation

CHALLENGES AND SOLUTIONS

CHALLENGES

Signal integrity

Ensure interoperability

Time-to-market Pressure

SOLUTIONS

New definition of specification

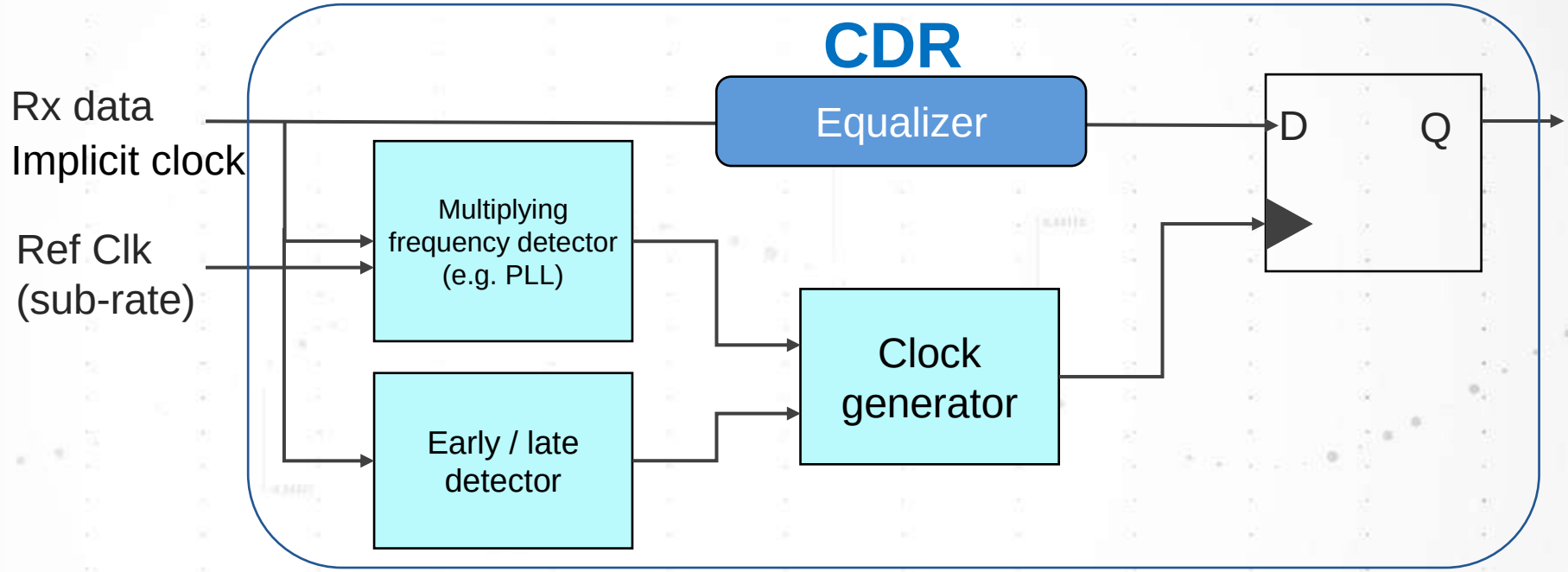
Leadership in measurement methodologies

Test Automation Software

DDR Rx Compared to High Speed Serial

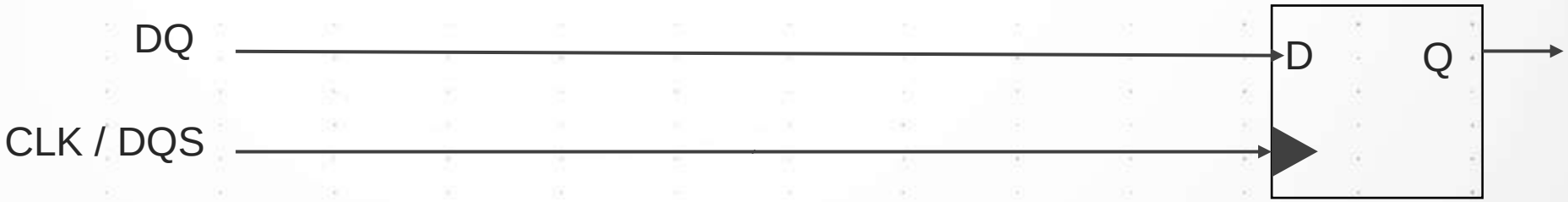
High Speed Serial

Complex



DDR Memory

Simple

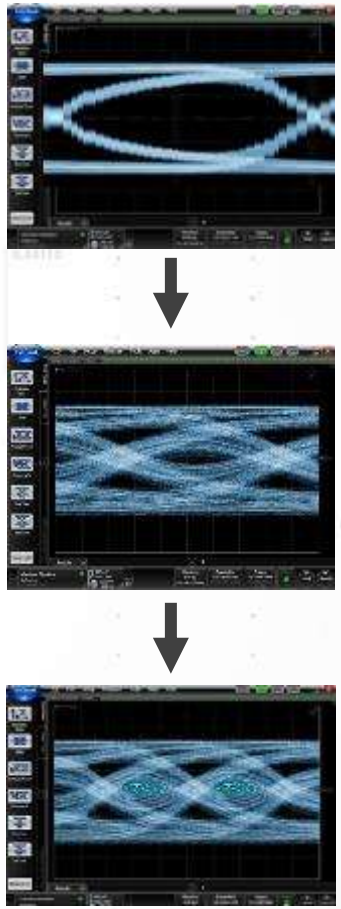


Shrinking Margins

NEW RX DEFINITION IN THE SPECIFICATION

Characteristics of DDR5 signals

- The data signals are wide and single-ended
  - Increased emphasis on multi-channel Rx test impairments
- Bidirectional data
  - Specification impacts on both write and read training
- DQS (strobe) is bursty instead of a continuous clock
  - ISI impact differs on preamble, first bits and the rest of burst



1600 MT/s

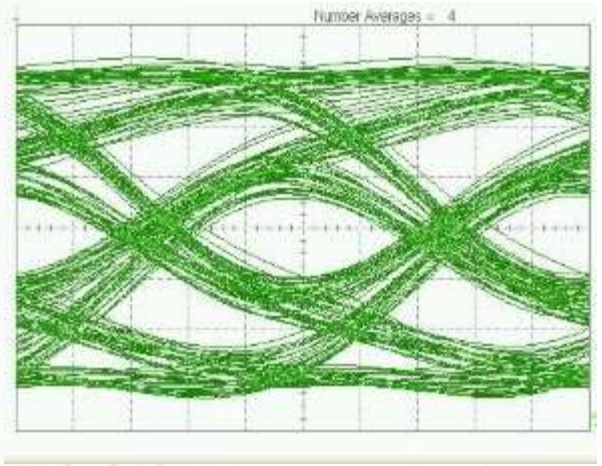
3200 MT/s

6400 MT/s

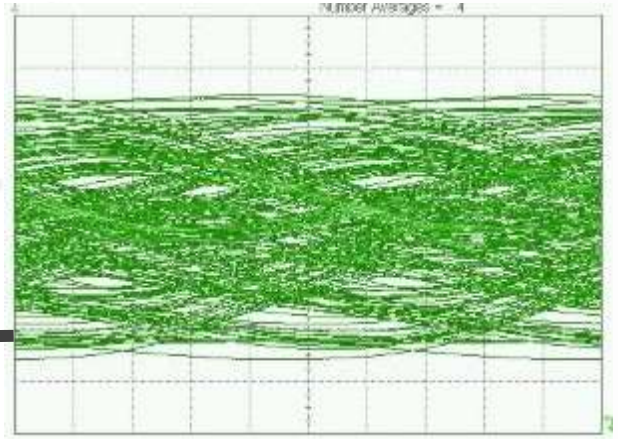
DDR5 is a New Game

EQUALIZATION NEEDED TO OPEN EYE

Open eye @ 3200Mbps



Closed eye @ 6400Mbps



DDR5 Memory

Not so Simple

Defining Measurement Requirements

PROVIDE LEADERSHIP IN NEW MEASUREMENTS

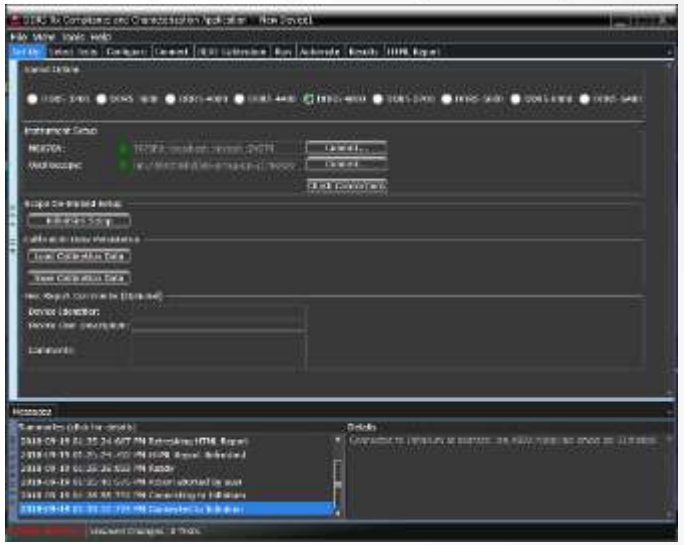
- Keysight and early technology adopters are working with the JEDEC standard in defining key Rx specifications

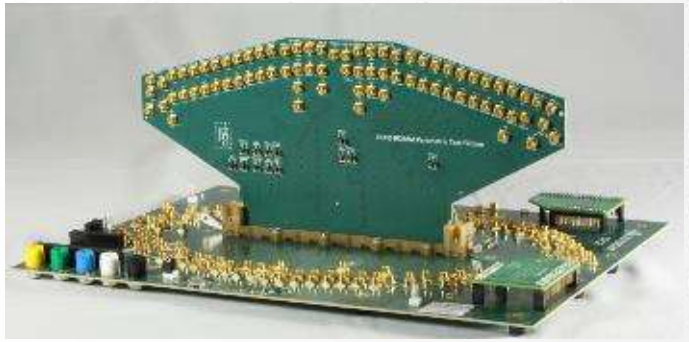
- Keysight is taking the leadership in:
  - Measurement requirements to characterize Rx parameters
  - Provide hardware and software requirements to enable full Rx testing capabilities

Time to Market Pressure

THE TOTAL SOLUTION APPROACH

- New Rx compliance test software
  - Amplitude, jitter, crosstalk, stressed eye, DFE calibration tests
  - Voltage, jitter sensitivity, and stressed eye tests
- Supports fixtures to complement Rx test requirements
  - Channel test card
  - Channel modelling board
  - Device and Parametric DIMM test card
- Seamless connection to data repository for quick test result analysis and decision making process

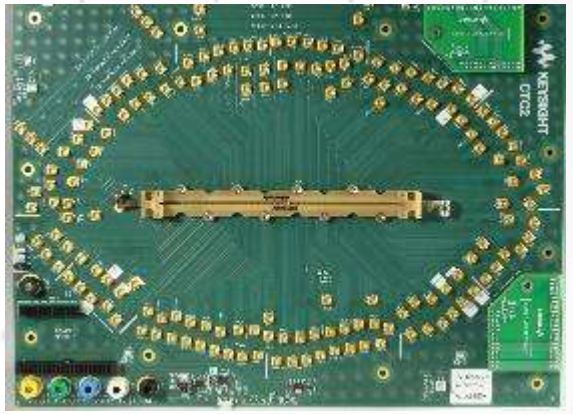




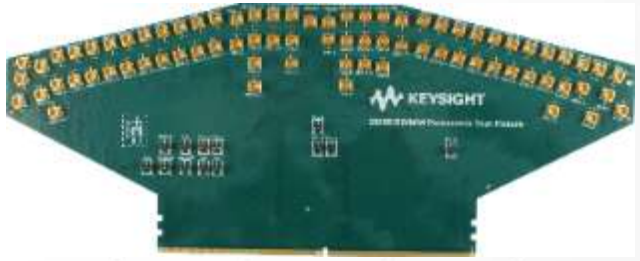
Test Fixtures

KEY COMPONENTS TO RX TEST

- **Channel Test Card - CTC2**
  - Socket for plugging in DIMM test card for calibration, DIMM module to be tested, or device test board
  - SMP connectors to provide access to CA/CTRL, strobe, and data
- **ISI board**
  - Contains different length standard compliant channels
- **Device Test Card**
  - Plugs into CTC and can be used by memory/register manufacturers to test their chips
- **Fully Passive DIMM Test Card**
  - Plugs into CTC
  - Signal breakout board for clock, CA, CTRL, strobe, and data
  - Used for signal inspection and Rx stress signal calibration
  - Signals are routed to SMP connectors

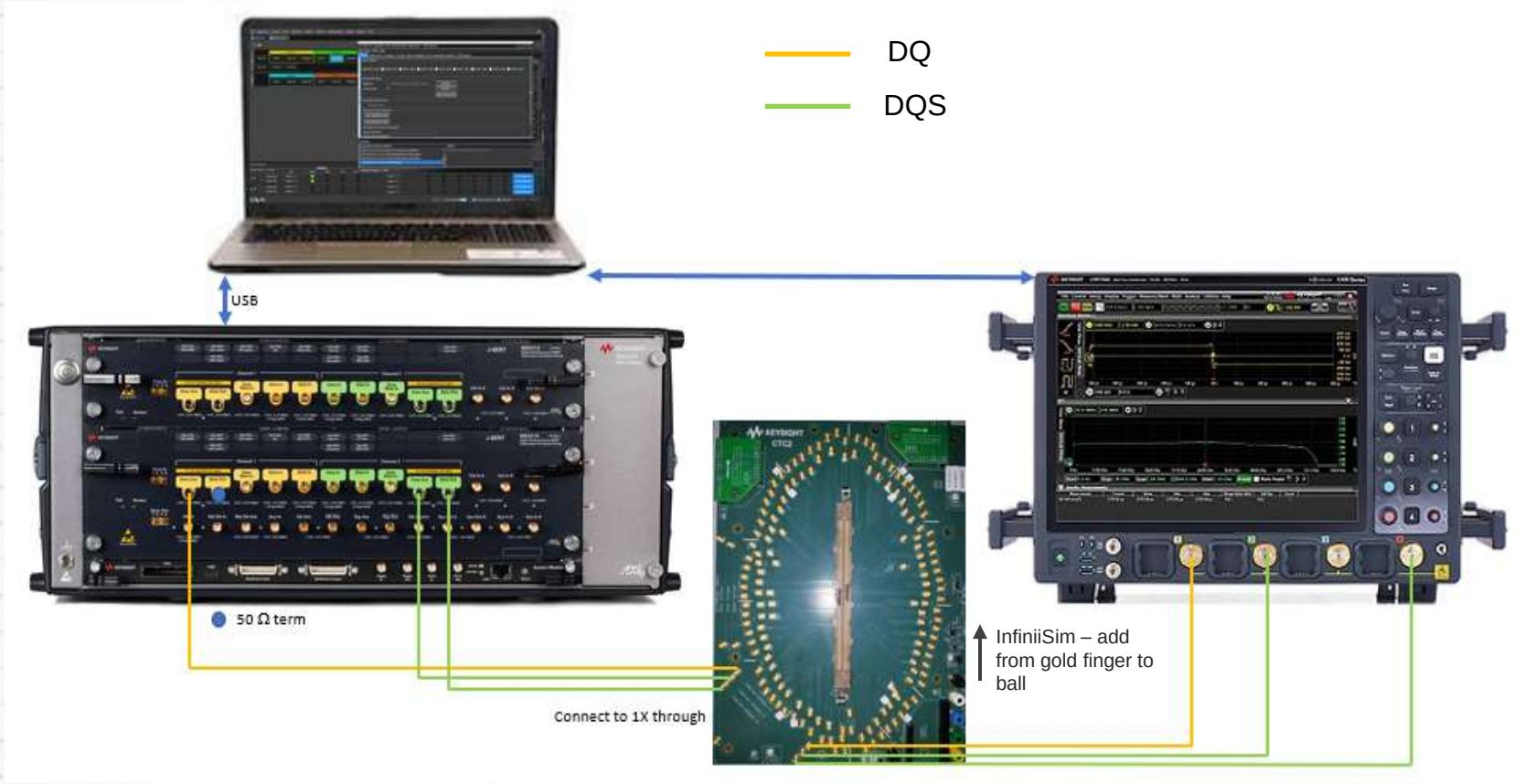


CTC2



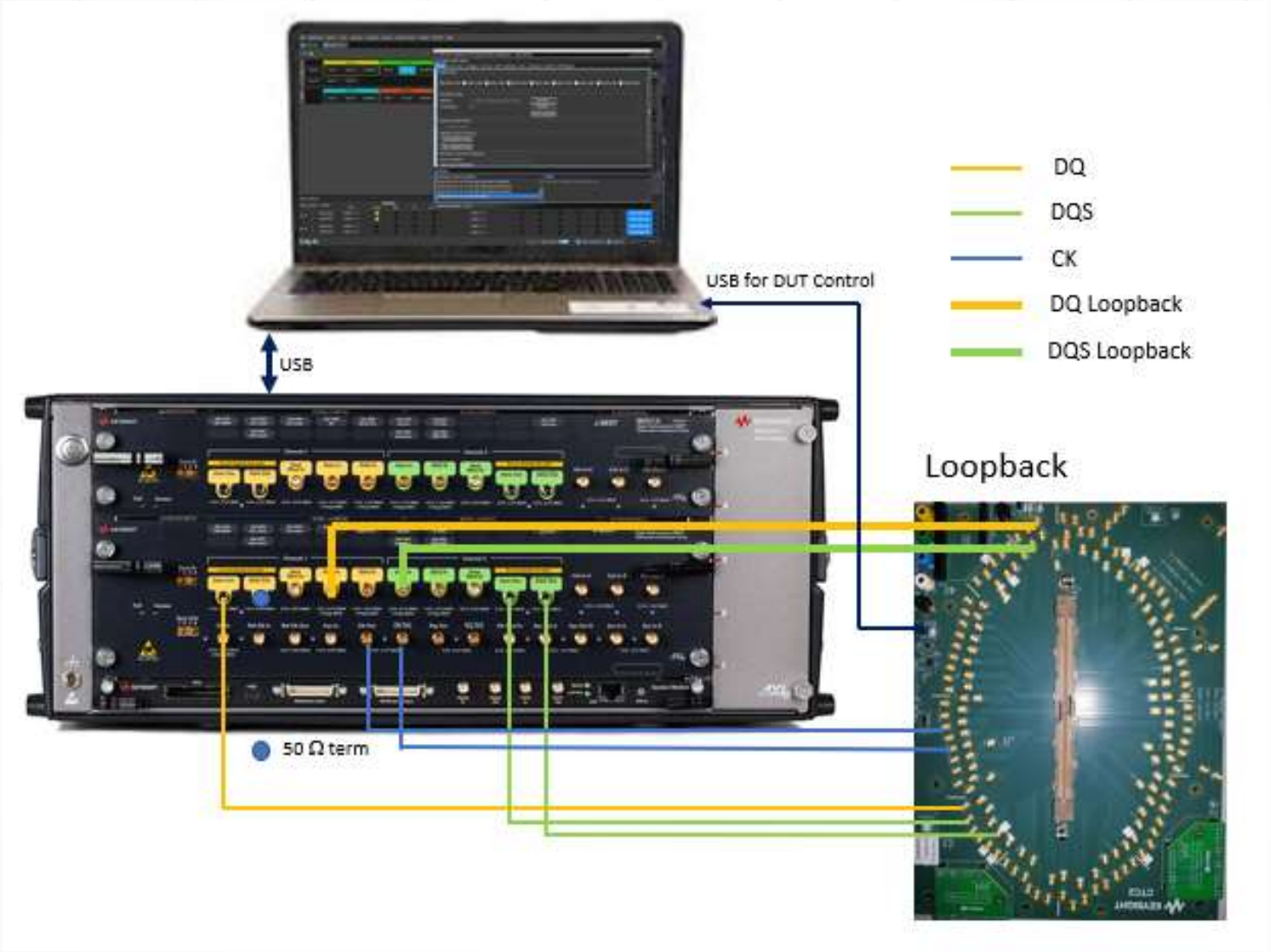
DIMM Test Card

Calibration Connection Diagram - RDIMM

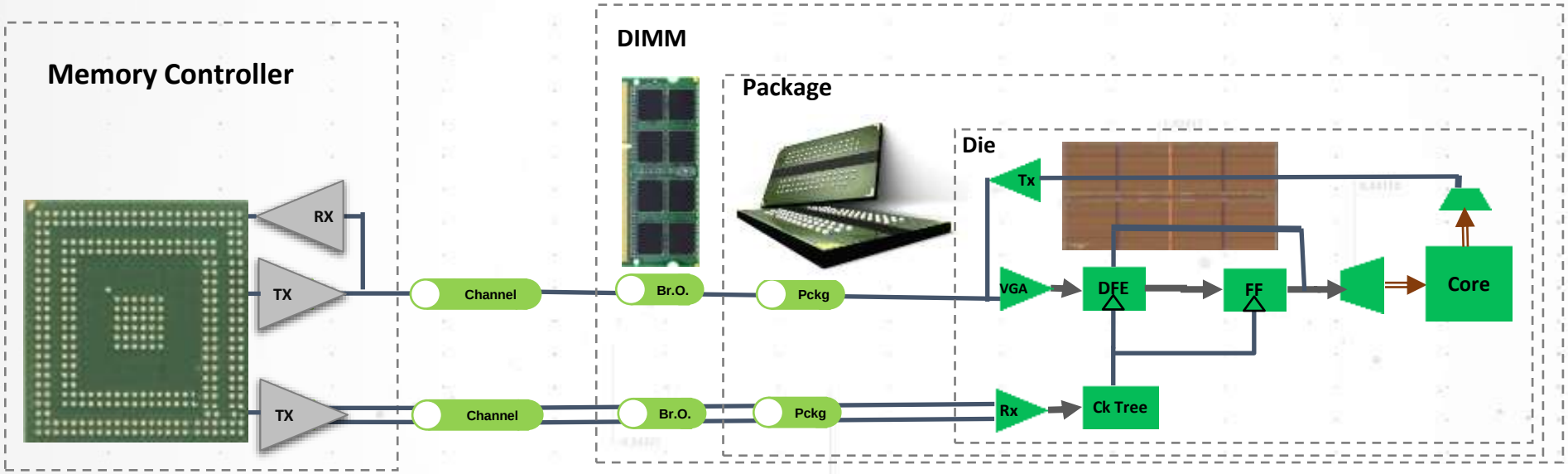


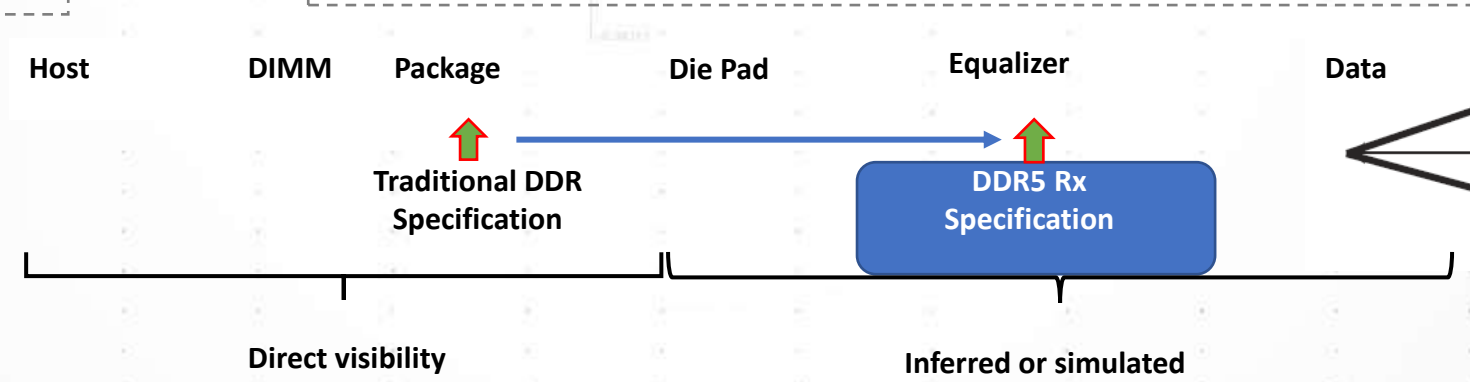
- Scope is a reference receiver

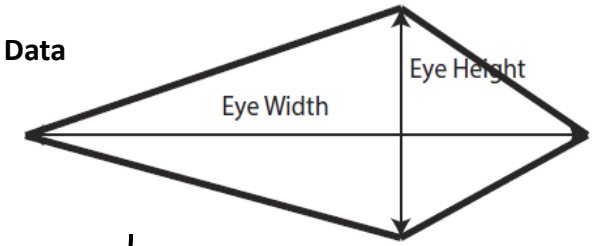
Test and Characterization Diagram (DQS/DQ)



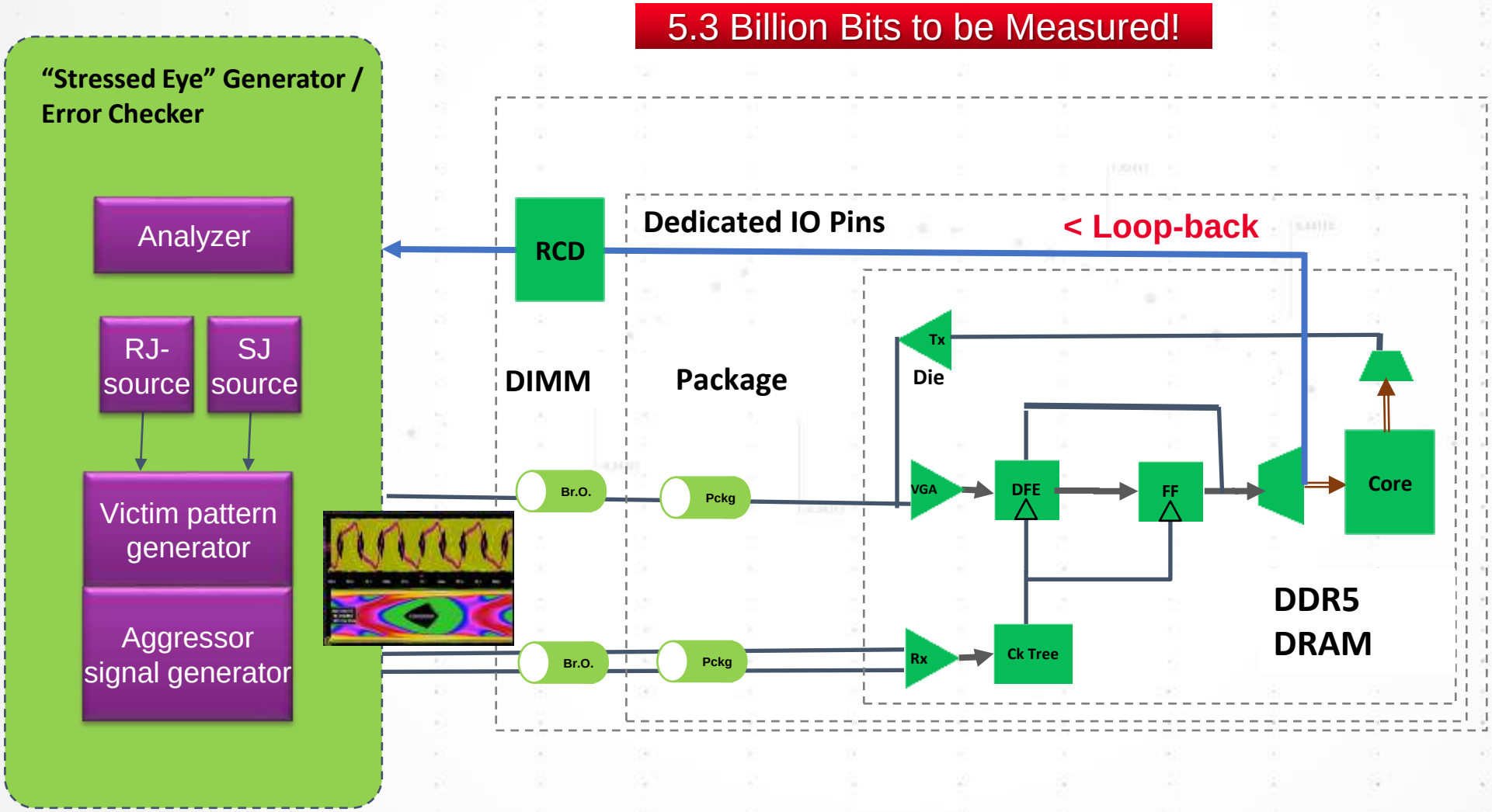
DDR5 Rx Specifications are now Inside the Die





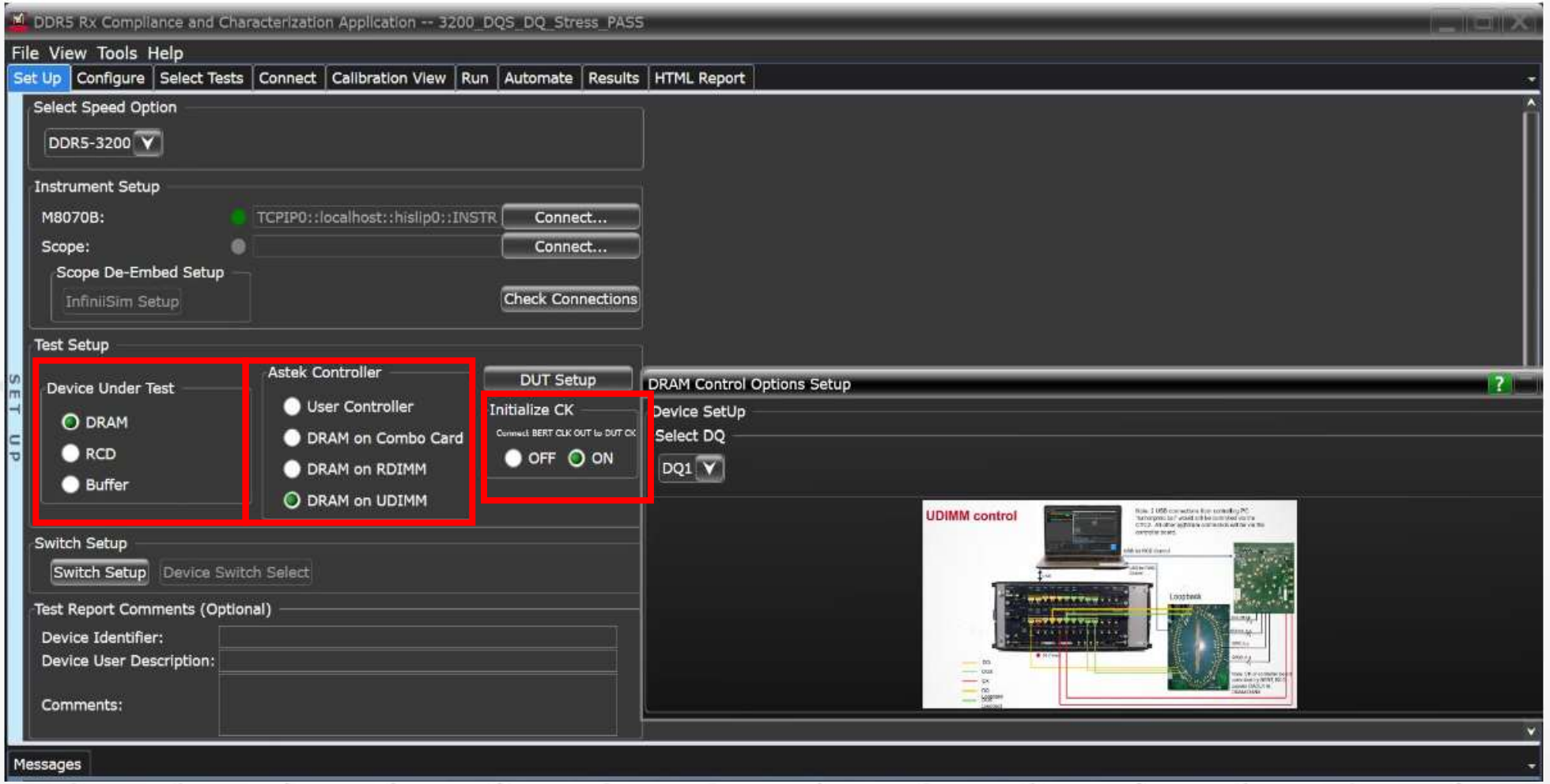


Accurate DDR5 Rx Specifications via Loop-Back Mode



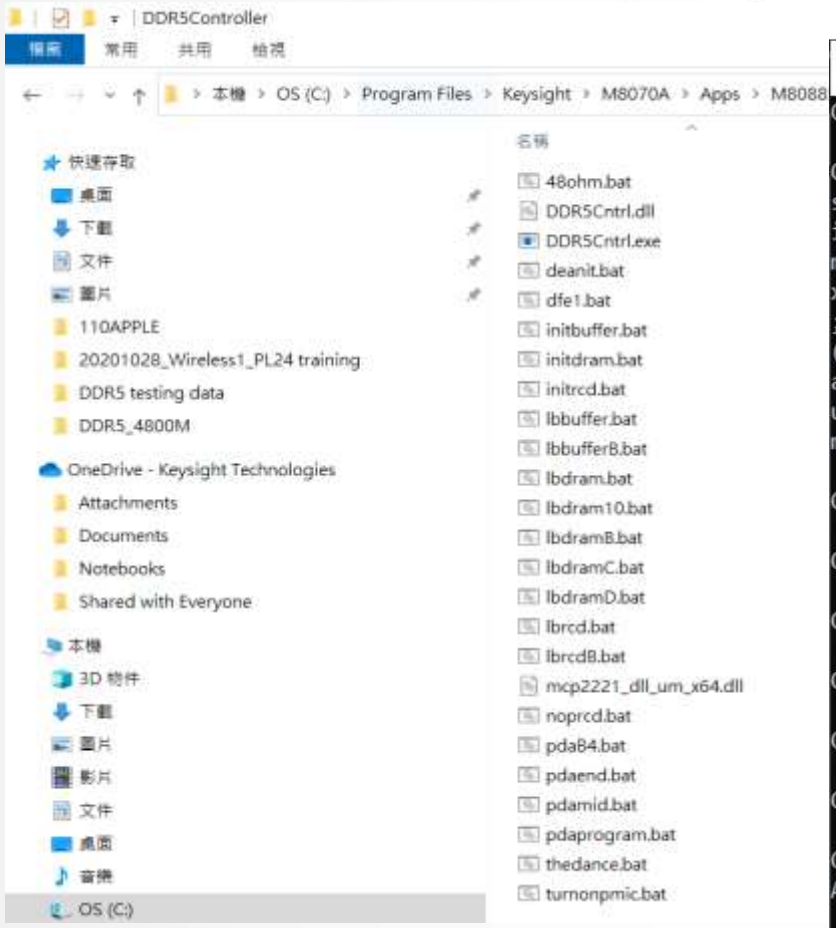
DDR5 RX M80555RCA Calibration/Testing software

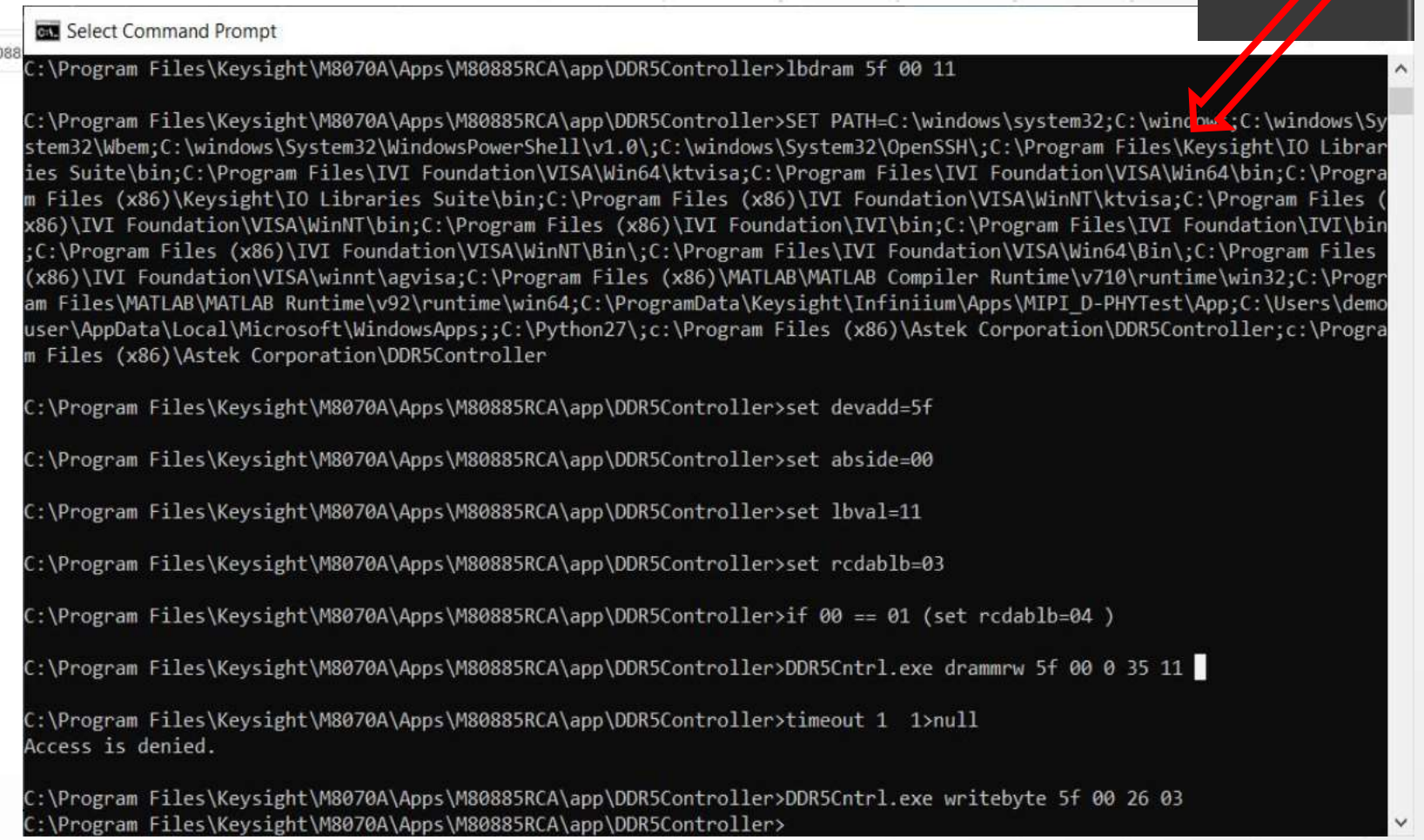
M80885A GUI



DDR5 RX DUT initializing/Loopback CML

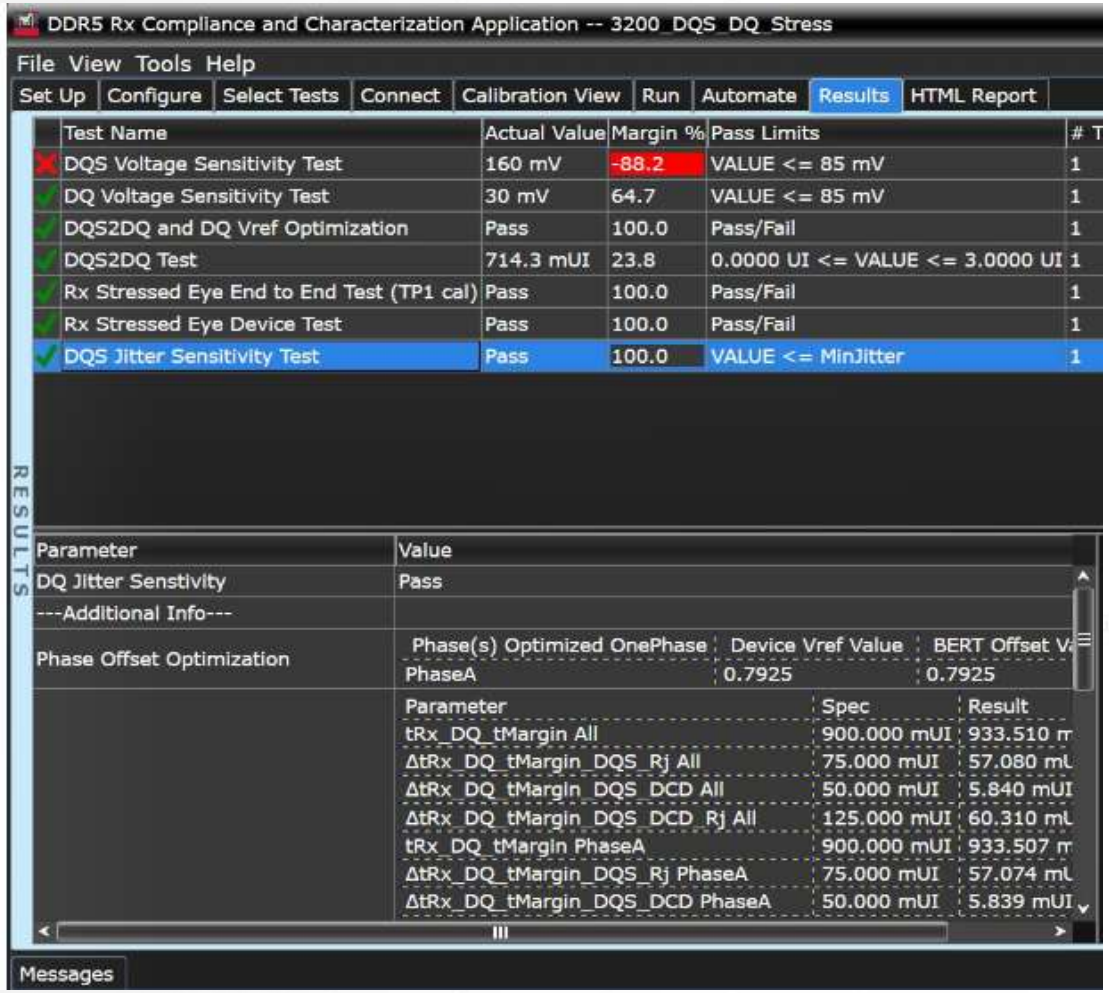
Initialize CK to make DUT initializing

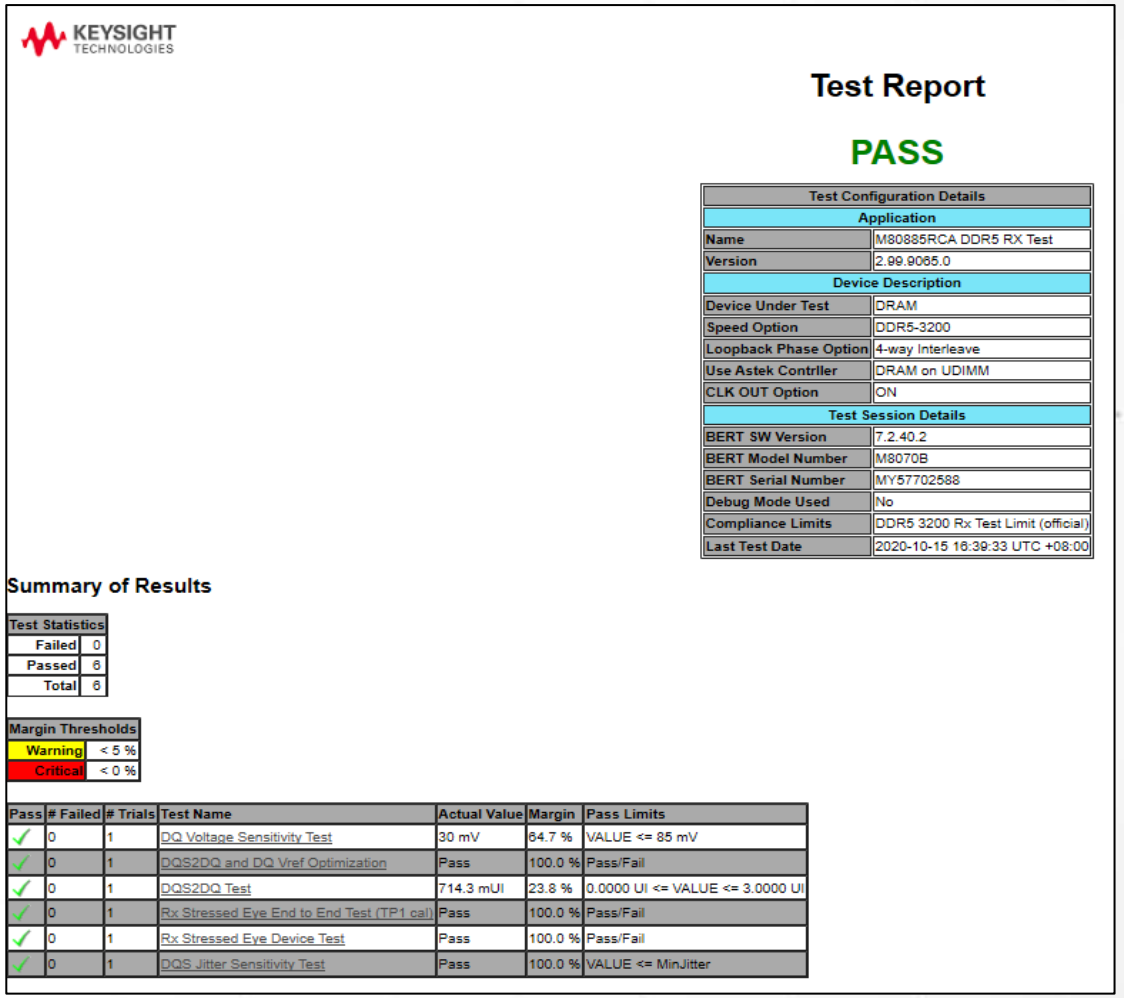




DDR5 3200M RX Testing Report

Keysight Standard Report





DDR5 3200M RX DQS Jitter Sensitivity

✓DQS Jitter Sensitivity Test

Test Summary: Pass | Test Description: DQS Jitter Sensitivity Test

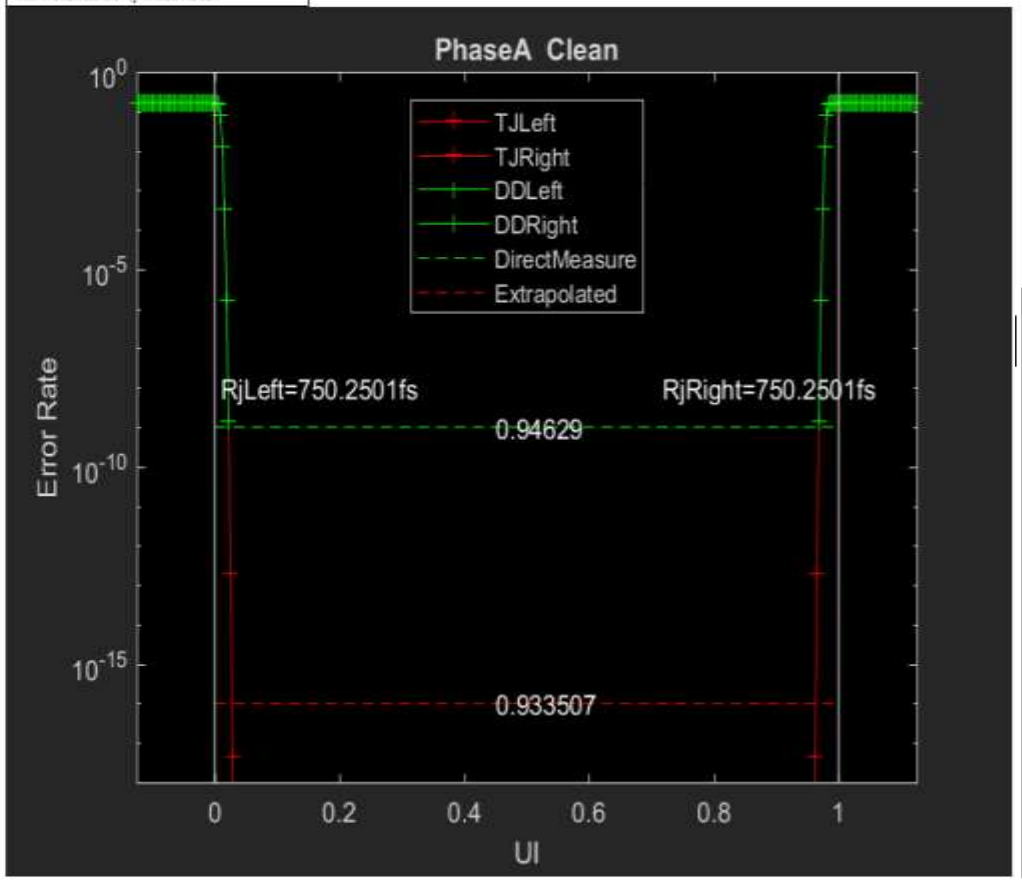
Pass Limits: <= MinJitter | DQ Jitter Sensitivity | Pass

Result Details

Phase Offset Optimization	(See table)	DQS Jitter Sensitivity Test Results	(See table2)	Jitter Sensitivity PhaseA Clean	(See image)	Jitter Sensitivity PhaseA Rj	(See image)	Jitter Sensitivity PhaseA DCD	(See image)	Jitter Sensitivity PhaseA Both	(See image)	PassLimit Max (MinJitter)	0.000

Trial 1

Trial 1: Jitter Sensitivity PhaseA Clean



Phase Offset Optimization

DQS Jitter Sensitivity Test Results

DQS Jitter Sensitivity Test Results

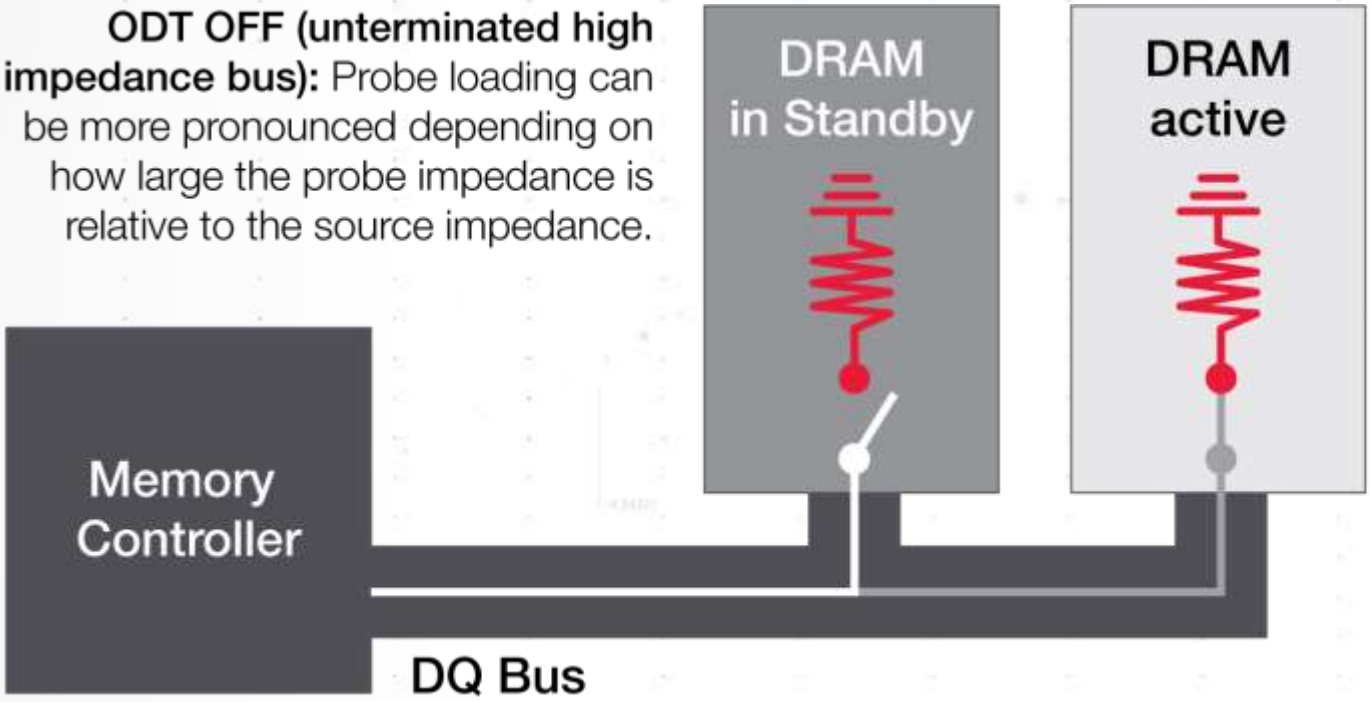
Parameter	Spec	Result	Status
tRx_DQ_tMargin All	900.000 mUI	933.510 mUI	Pass
Rx_DQ_tMargin_DQS_Rj All	75.000 mUI	57.080 mUI	Pass
Rx_DQ_tMargin_DQS_DCD All	50.000 mUI	5.840 mUI	Pass
Rx_DQ_tMargin_DQS_DCD_Rj All	125.000 mUI	60.310 mUI	Pass
tRx_DQ_tMargin PhaseA	900.000 mUI	933.507 mUI	Pass
Rx_DQ_tMargin_DQS_Rj PhaseA	75.000 mUI	57.074 mUI	Pass
Rx_DQ_tMargin_DQS_DCD PhaseA	50.000 mUI	5.839 mUI	Pass
Rx_DQ_tMargin_DQS_DCD_Rj PhaseA	125.000 mUI	60.306 mUI	Pass
tRx_DQ_tMargin PhaseB	900.000 mUI	1.000000 UI	Pass
Rx_DQ_tMargin_DQS_Rj PhaseB	75.000 mUI	1.000000 UI	Pass
Rx_DQ_tMargin_DQS_DCD PhaseB	50.000 mUI	1.000000 UI	Pass
Rx_DQ_tMargin_DQS_DCD_Rj PhaseB	125.000 mUI	1.000000 UI	Pass
tRx_DQ_tMargin PhaseC	900.000 mUI	1.000000 UI	Pass
Rx_DQ_tMargin_DQS_Rj PhaseC	75.000 mUI	1.000000 UI	Pass
Rx_DQ_tMargin_DQS_DCD PhaseC	50.000 mUI	1.000000 UI	Pass
Rx_DQ_tMargin_DQS_DCD_Rj PhaseC	125.000 mUI	1.000000 UI	Pass
tRx_DQ_tMargin PhaseD	900.000 mUI	1.000000 UI	Pass
Rx_DQ_tMargin_DQS_Rj PhaseD	75.000 mUI	1.000000 UI	Pass
Rx_DQ_tMargin_DQS_DCD PhaseD	50.000 mUI	1.000000 UI	Pass
Rx_DQ_tMargin_DQS_DCD_Rj PhaseD	125.000 mUI	1.000000 UI	Pass

DDR5 and LPDDR5 Probing Challenges and Solutions

DDR Memory On-die Termination Modes

PROBE INPUT IMPEDANCE RELATIVE TO SOURCE

ODT OFF (unterminated high impedance bus): Probe loading can be more pronounced depending on how large the probe impedance is relative to the source impedance.

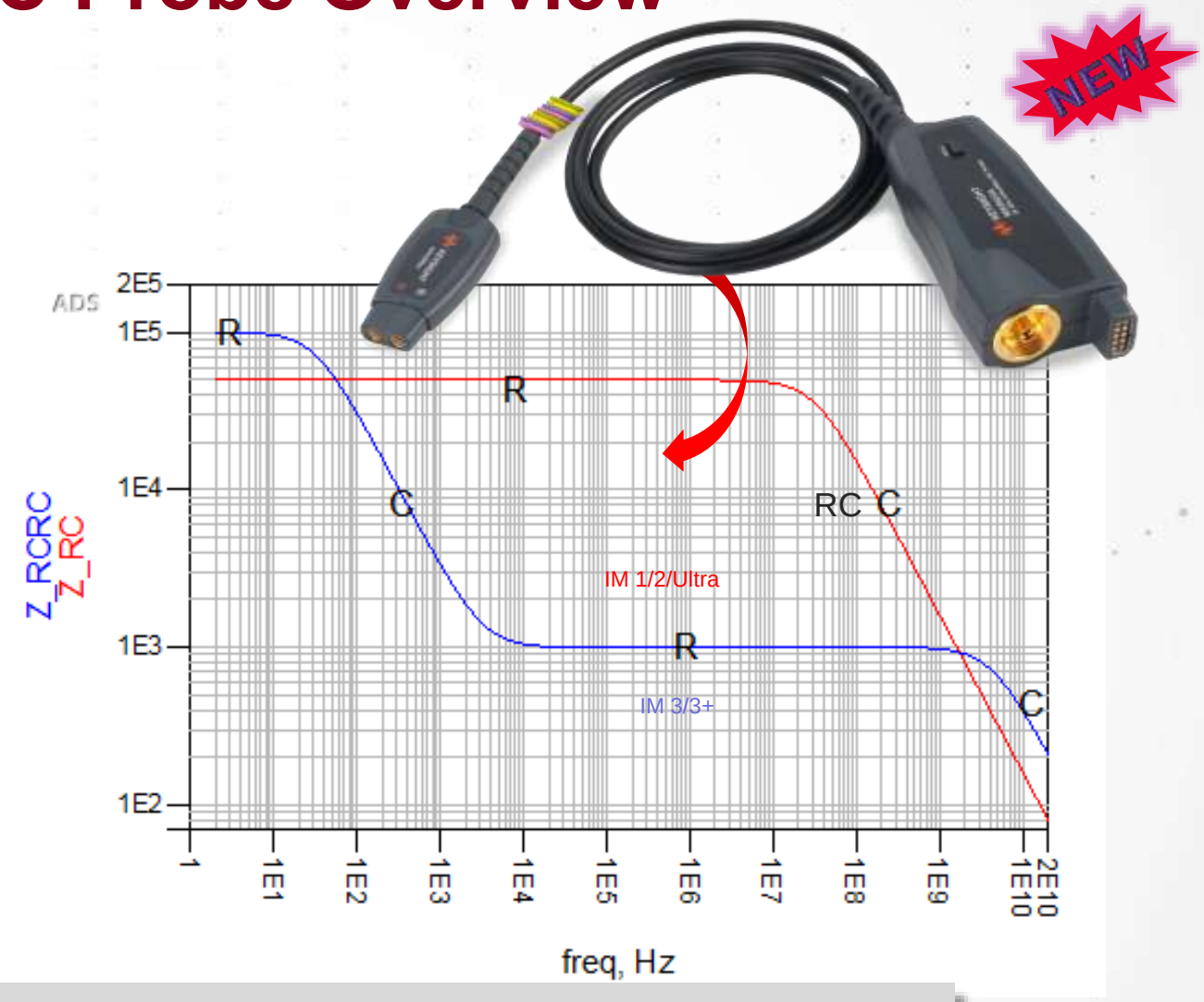


ODT ON (low impedance bus): The source impedance dominates loading.

Dynamic ODT enables the DRAM to switch between high or low termination impedance. When the termination impedance goes high, probe impedance needs to be high enough to reduce probe loading.

Ultra InfiniiMax 25 GHz RC Probe Overview

- 25 GHz (with MX0100A micro head)
- AutoProbe II interface – direct plug-in to UXR Jr, V, Q, 90kX
- RC input impedance profile with low midband loading
  - 25 k ohm input R @DC each signal to ground
  - 0.17 pF input C when used with MX0100A
- Compatible with most of InfiniiMax I/II probe head accessories



"RC" (red trace): traditional resistance – then capacitance impedance
"RCRC" (blue trace): High DC impedance, moderate mid-band

RC vs RCRC Probe For Probing LPDDR4 Signal

RC probe is a better choice when probing buses that transition to a “high Z” state or when dealing with signal with high impedance.

Measured with RCRC probe (N7003A)

Measured with RC probe (1169B)

New PoP/BGA Interposers for DDR5 and LPDDR5

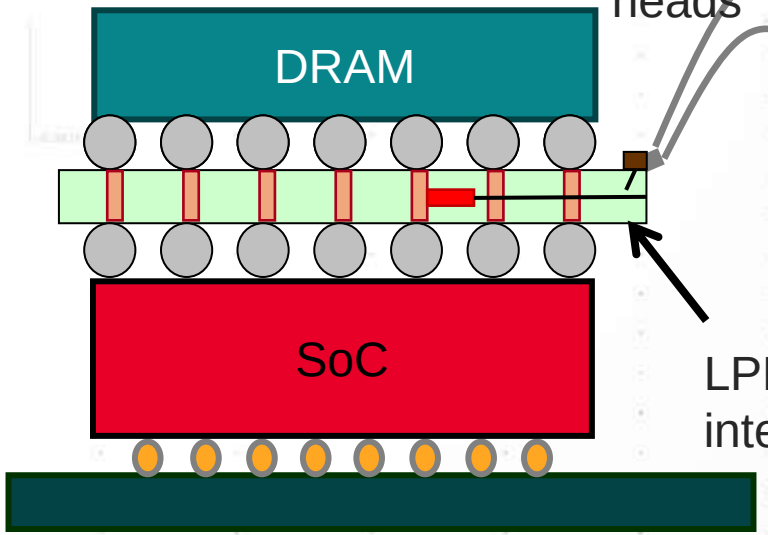
CRITICAL FOR TX AND PROTOCOL SOLUTIONS

- Previous generation BGA/PoP interposer design/materials don't cover DDR5/LPDDR5 data rates.
- New BGA/PoP interposer designs characteristics:
  - Thinner (previously 70 mils, **new 20 – 22 mils**)
  - New materials and processes.
    - Improved SI
    - Decreased crosstalk
  - Integrated Riser + Interposer
    - Better performance than separate parts
    - Easier attachment to DUT
    - Available on custom probes

UXR scope

MX0100 micro probe heads

25 GHz probe



LPDDR5 PoP interposer

thinner

DDR5 Protocol Design Test and Validation

CHALLENGES AND SOLUTIONS*

CHALLENGES

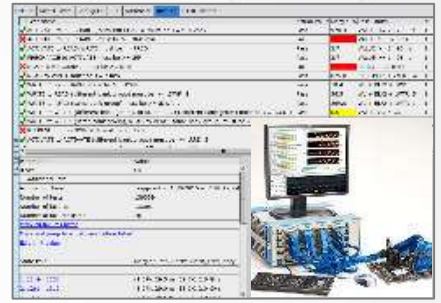
Ensure interoperability

Identify root cause of system failure

Time-to-market Pressure

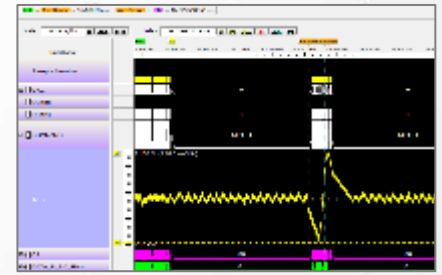
SOLUTIONS

Protocol Compliance and validation



Debug with complete view of the DDR traffic using powerful analysis tools

Viewscope to visualize noise on power or signal integrity issues correlated to memory analysis



* DDR5 data rate coverage will vary by system under test and logic analysis solution.

Ensure Interoperability

PROTOCOL COMPLIANCE AND DATA VALIDATION

Test

- Test and monitor your system under variable conditions

Functional Compliance Validation

- Validate system is within JEDEC specifications
  - Quick pass/fail results
  - Includes margin information on how far the system is deviating from the ‘pass limits’
  - Includes number of times violation occurred and how many times violation was tested

- If not…..risk of system failures

RESULTS

	Test Name	Actual Value	Margin %	Pass Limits
✓	ACTIVATE to PRECHARGE/Auto-PRECHARGE must be <= tRASmax	Pass	101E+02	VALUE <= 70.200 µs
✓	ACTIVATE to PRECHARGE must be >= tRASmin	Pass	68.2	max(42ns, 3CK)
✓	ACTIVATE to READ/WRITE must be >= tRCD	Pass	0.4	max(18ns, 4CK)
✗	ACTIVATE to ACTIVATE (different banks) must be >= tRRD	Fail	-0.8	max(10ns, 4CK)
✓	Four ACTIVATE window (different banks) must be >= tFAW	Pass	0.0	VALUE >= 40.0 ns
✓	MRW command to MRW command (or CKE low) must be > tMRW	Pass	40.0	max(10ns, 10CK)
✓	MRW command to any valid command must be > tMRD	Pass	20.0	max(14ns, 10CK)
✓	MRR command to any valid command (or CKE low) must be > tMRR	Pass	375.0	VALUE >= 8 CK
✓	PRECHARGE (all banks) to ACTIVATE/REFRESH must be >= tRPab	Pass	1.1	max(21ns,3CK)
✓	PRECHARGE (per bank) to ACTIVATE/REFRESH must be >= tRPpb	Pass	302E+01	max(18ns,3CK)
✓	Duration of CKE high/low >= tCKE.	Pass	34.4	max(7.5ns,4CK)

Parameter	Value
tRRD	Fail
---Additional Info---	
Acquisition Time	Triggered on 10/3/2016 at 7:41:03 PM
Number of tests	118872
Number of failures	421
Number of failures listed	20
Mark all failures listed	
Mark and jump to worst case failure listed	
Edit limit value	

Violation detection across speed changes

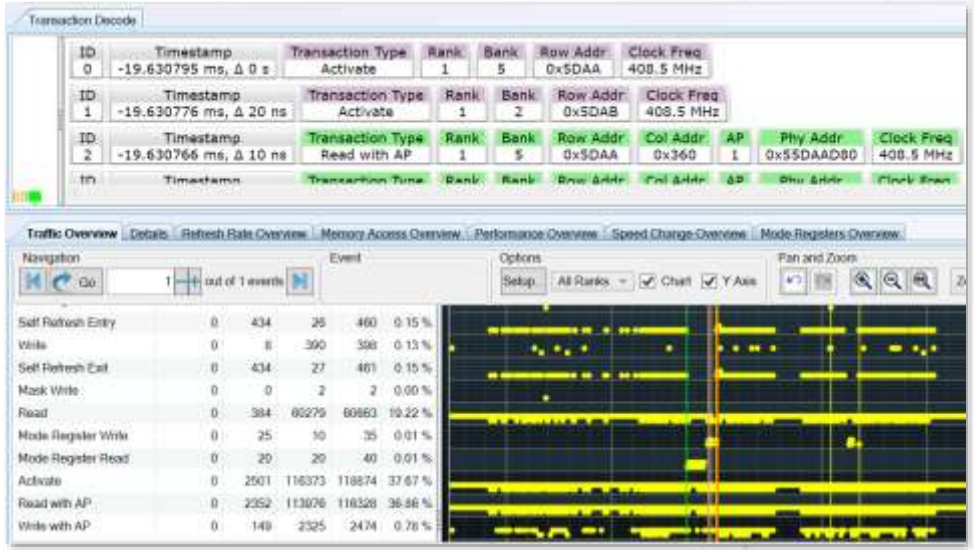
Identify Root Cause of System Failure

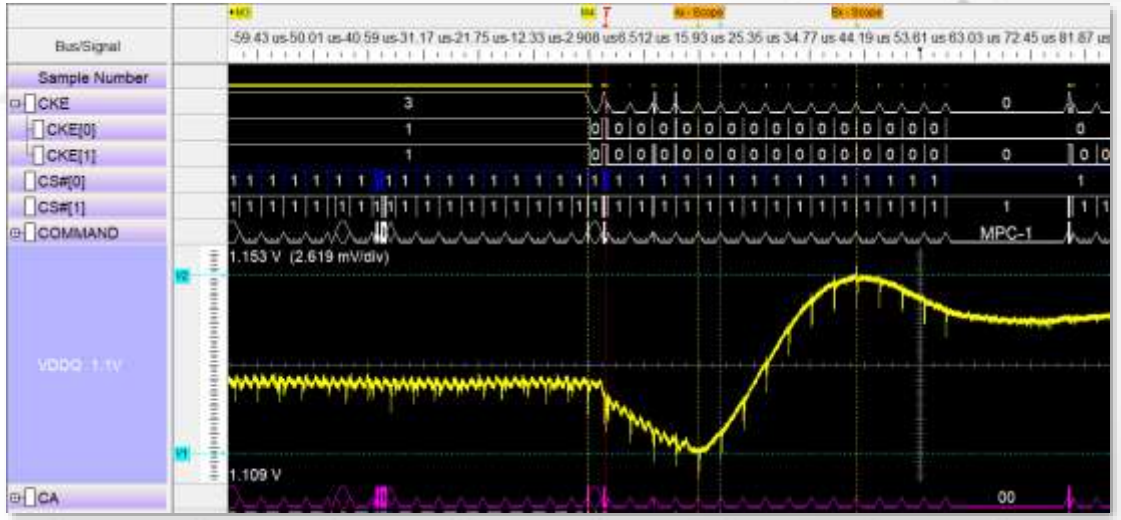
DEBUG CAPABILITIES

Something is wrong with your system

- Check the flow of the traffic between the memory controller and memory device to get to the root cause of system issues

- Correlate memory traffic to scope capture of:
  - Signal integrity of specific signals
  - Power integrity

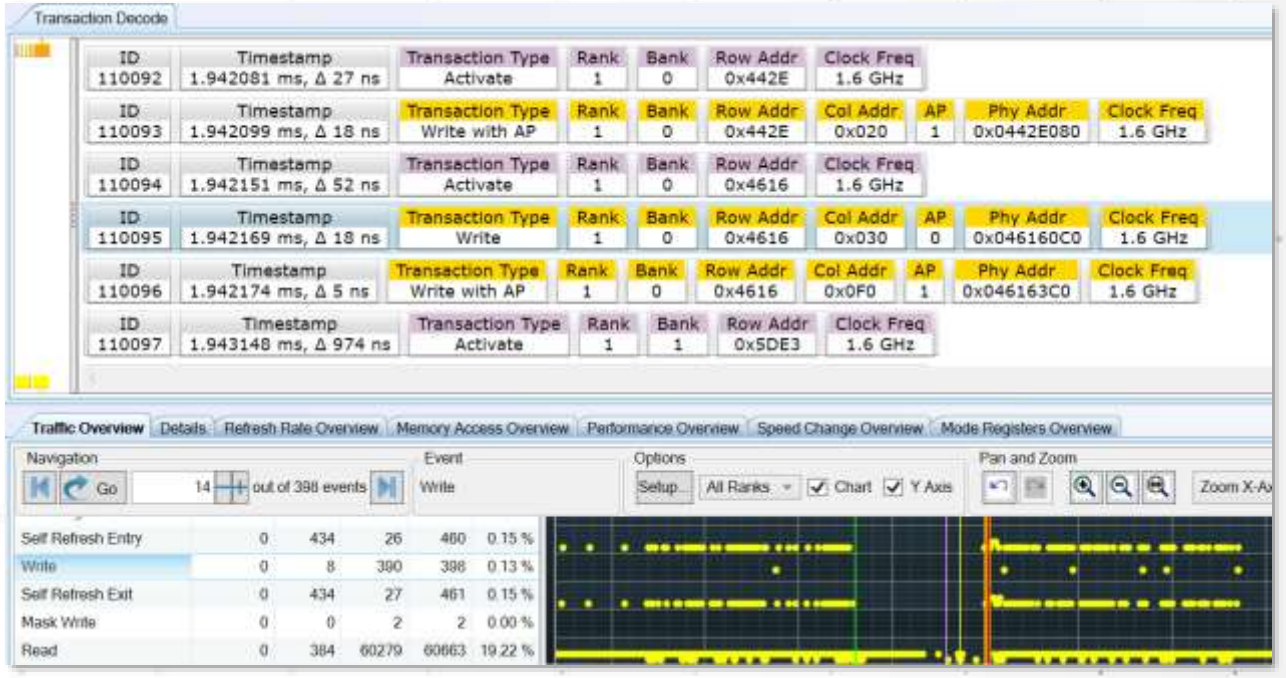




Time to Market Pressure

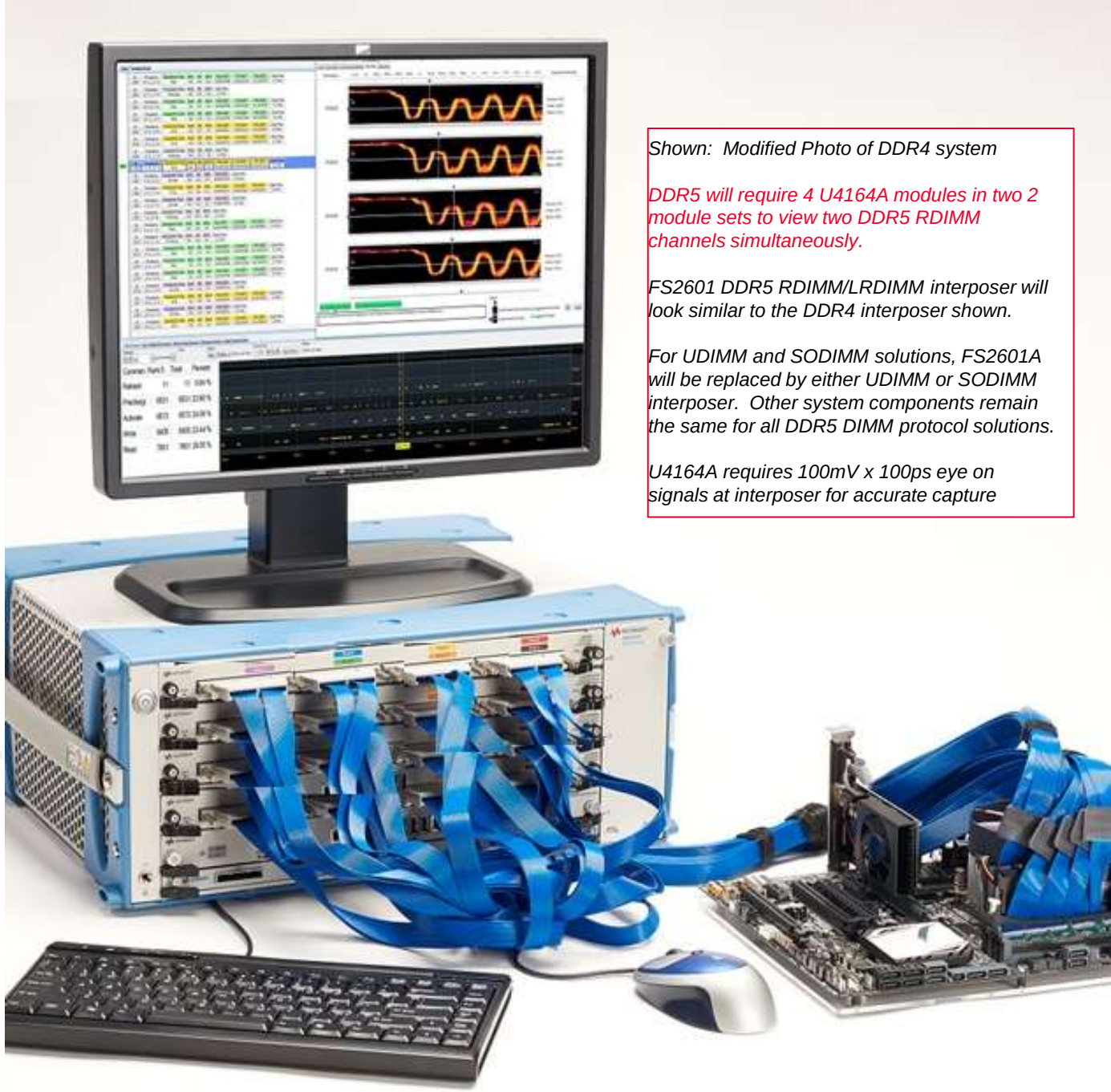
ANALYSIS SW TOOLS ACCELERATE INSIGHT

- Rapid Navigation with Traffic Overview, Transaction Decode, Details tab, Refresh Overview, Memory Access Overview, Performance Overview, Mode Register Overview, and Speed Change Overview
- See when events happened
- Follow signal flow and understand, “What happened?”
- Compliance testing to locate potential failures



DDR5 configuration for RDIMM or LRDIMM

- Qty (4) U4164A logic analyzer modules qty (2) sets of 2 modules
  - Qty (4) option -02G speed grade option
  - Qty (4) optional customer choice of memory depth options
- Qty (1) M9505A chassis
- Qty (1) M9537A embedded controller
- Qty (1) FS2600 or FS2604 DDR5 RDIMM/LRDIMM Interposer
- Qty (1) B4661A Memory Analysis SW
  - Qty (1) B4661A-5FP/5TP/5NP
    DDR5 Analysis and Compliance Validation



Shown: Modified Photo of DDR4 system

DDR5 will require 4 U4164A modules in two 2 module sets to view two DDR5 RDIMM channels simultaneously.

FS2601 DDR5 RDIMM/LRDIMM interposer will look similar to the DDR4 interposer shown.

For UDIMM and SODIMM solutions, FS2601A will be replaced by either UDIMM or SODIMM interposer. Other system components remain the same for all DDR5 DIMM protocol solutions.

U4164A requires 100mV x 100ps eye on signals at interposer for accurate capture

Looking Ahead – DDR6*

- DDR5 started in 2016
  - Typical 5 year spec development process
- Expect DDR6 spec development late 2022, early 2023
- Keysight DDR6 pathfinding
  - Crosstalk more focus
  - Fully closed eye specification
  - Double bandwidth with similar power budget
- Low noise UXR oscilloscope to meet jitter/eye limits
- M8040A BERT for NRZ/PAM4 signaling support

	DDR5	DDR6*
Capacity	8 GB	16 GB
Burst length	16	32
Max speed	8.4 GT/s	16.8 GT/s

* Keysight opinion, not official JEDEC specs or plans. Based on historical 2x performance improvements over similar channels

KEYSIGHT
TECHNOLOGIES